T5.4: Design, fabrication and characterization of controller circuit on 28nm and 14nm node [Leader: FhG IIS]

Start: M7

End: M40

Objectives:

O5.4: Develop testchip for high temperatures in nanometer CMOS

Status

- Testchip28 with test structures for logic, RAM and an ADC for very high temperature in 28 nm technology successfully designed, fabricated and evaluated at -40 to 200 ^{o}C
- Testchip14, testchip design and simulation in 14 nm with same logic as in testchip28 only due to the high production costs for 14 nm technologies
- SoC28 microcontroller design in 28 nm technology with MRAM and communication interfaces successfully designed, fabricated and evaluated at -40 to 200 ^{o}C

Testchip28

- Design of 3 stand alone sub-chip design on one die
- Testchip28-Logic
  - 12 different ring-oscillator/delay-line structures and I/O cells adapted for high temperature characterization (INV/NAND2/NOR2 gates, drive strength, loads)
- Testchip28-RAM
  - 1k x 32 bit RAM cell with memory BIST structures adapted for high temperature testing
- Testchip28-ADC12
  - 12-bit SAR ADC for testing analog behavior at high temperature
- Evaluation for all 3 sub-chips was done successfully in a temperature range of -40 to 200 ^{o}C

Testchip28 Layout

Testchip28 layout plot:

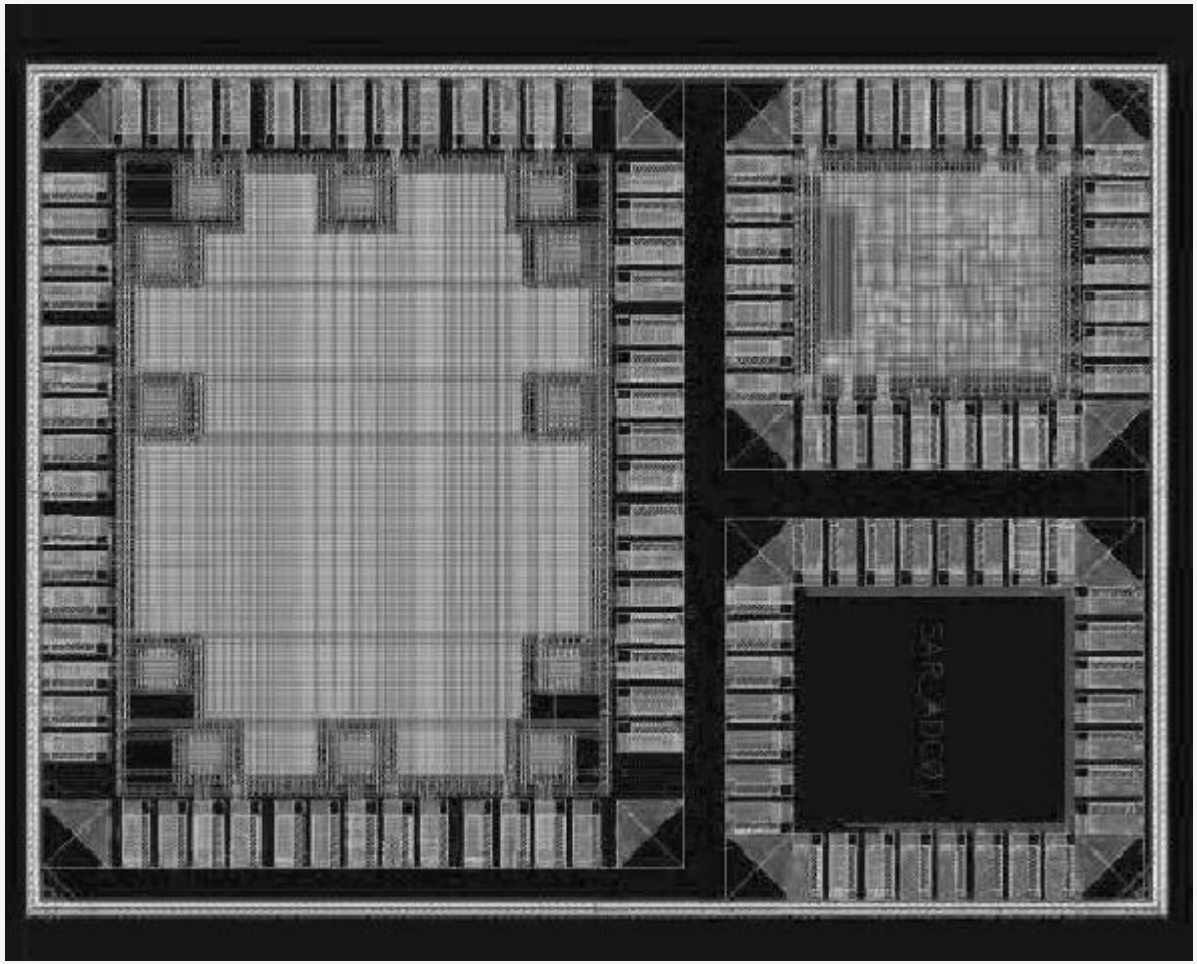
- Total chip area 3.6 mm2
- Pad limited design

Testchip triplet:

- Left:
- Testchip28-Logic

- Upper right:
- Testchip28-RAM

- Lower right:
- Testchip28-ADC12



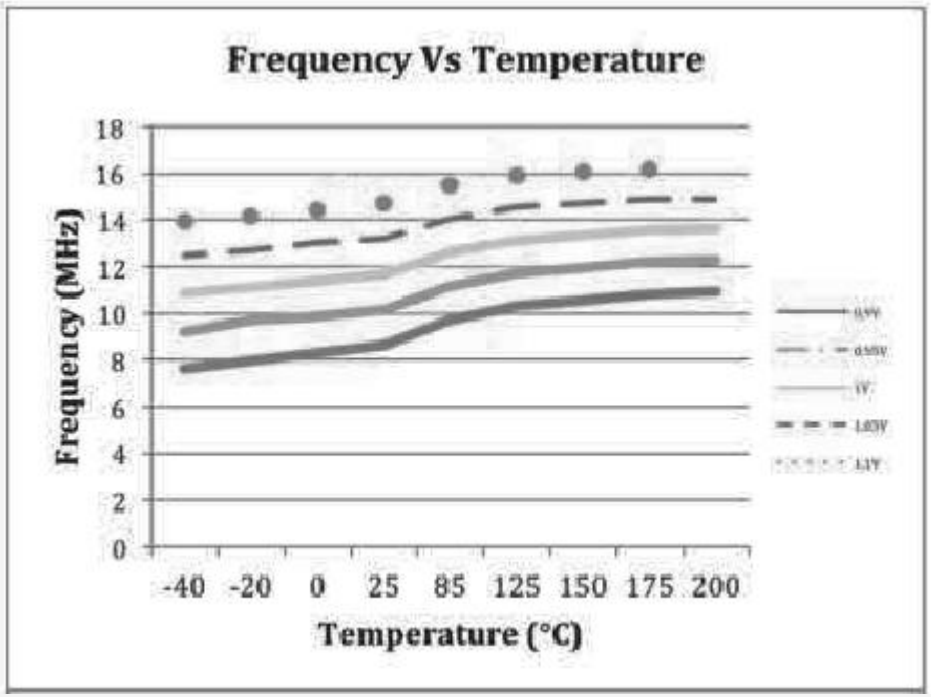
Testchip28 Evaluation

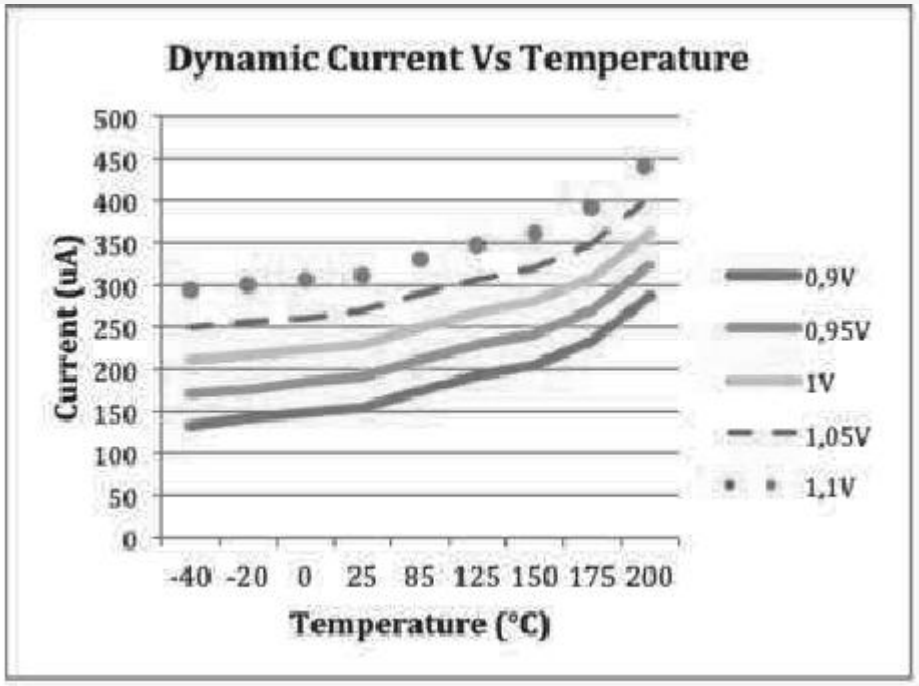
- Testchip28 evaluation with ATS 515 Thermostream®
- Temperature range -40 oC to +200 oC or Tmax
- Core voltage range -10%, -5%, typical 1 V, +5%, +10%
- I/O voltage typical 1.8V

- Measurements
  - Dynamic power
  - Leakage power
  - Output frequency ring oscillators (LOGIC)
  - All measurements were functionally correct over full temperature range

- Successful memory BIST (RAM) down to 0.68V

Testchip28 Evaluation

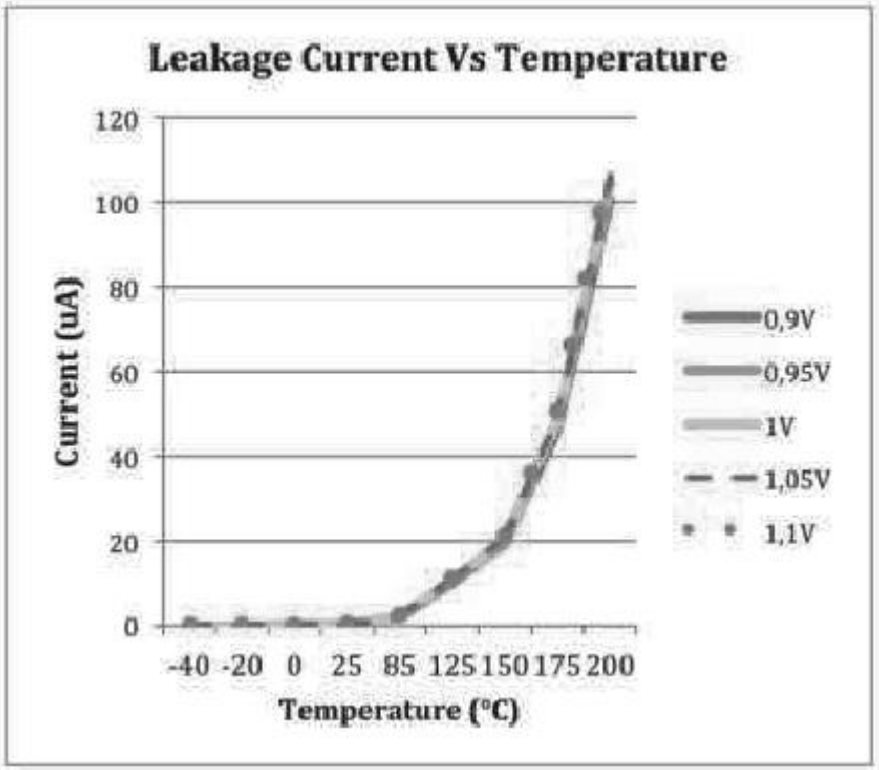




Temperature increase: delay impact depending on VDD and VT

More STA Corners to determine Worst Case variation (VDD,T)

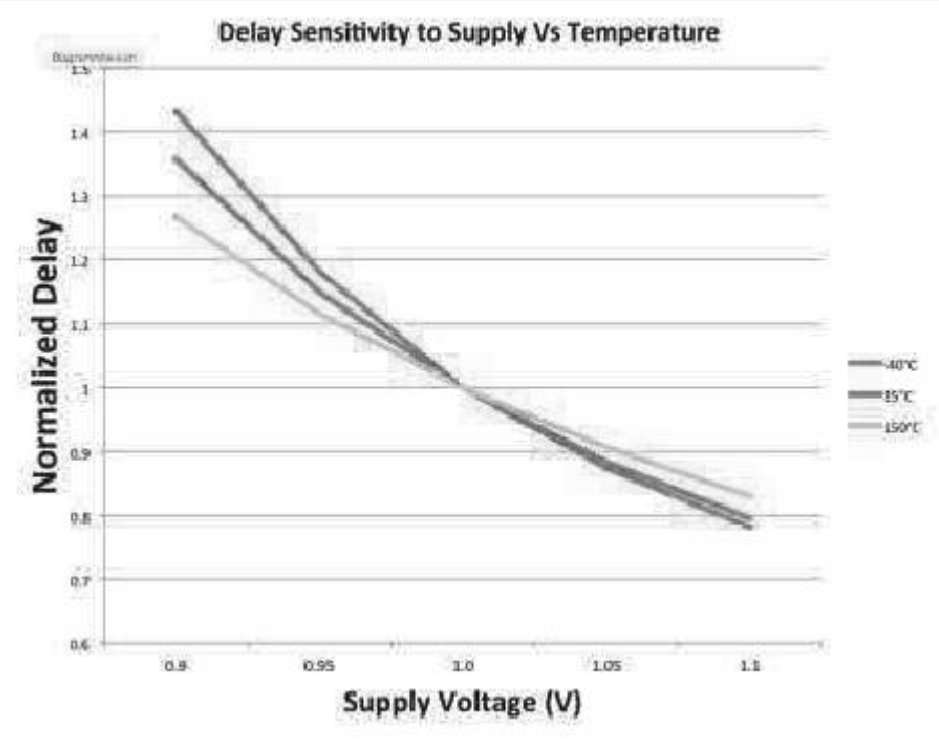
Testchip28 Evaluation



E.g. Leakage increase 8x from 25° C to 85° C

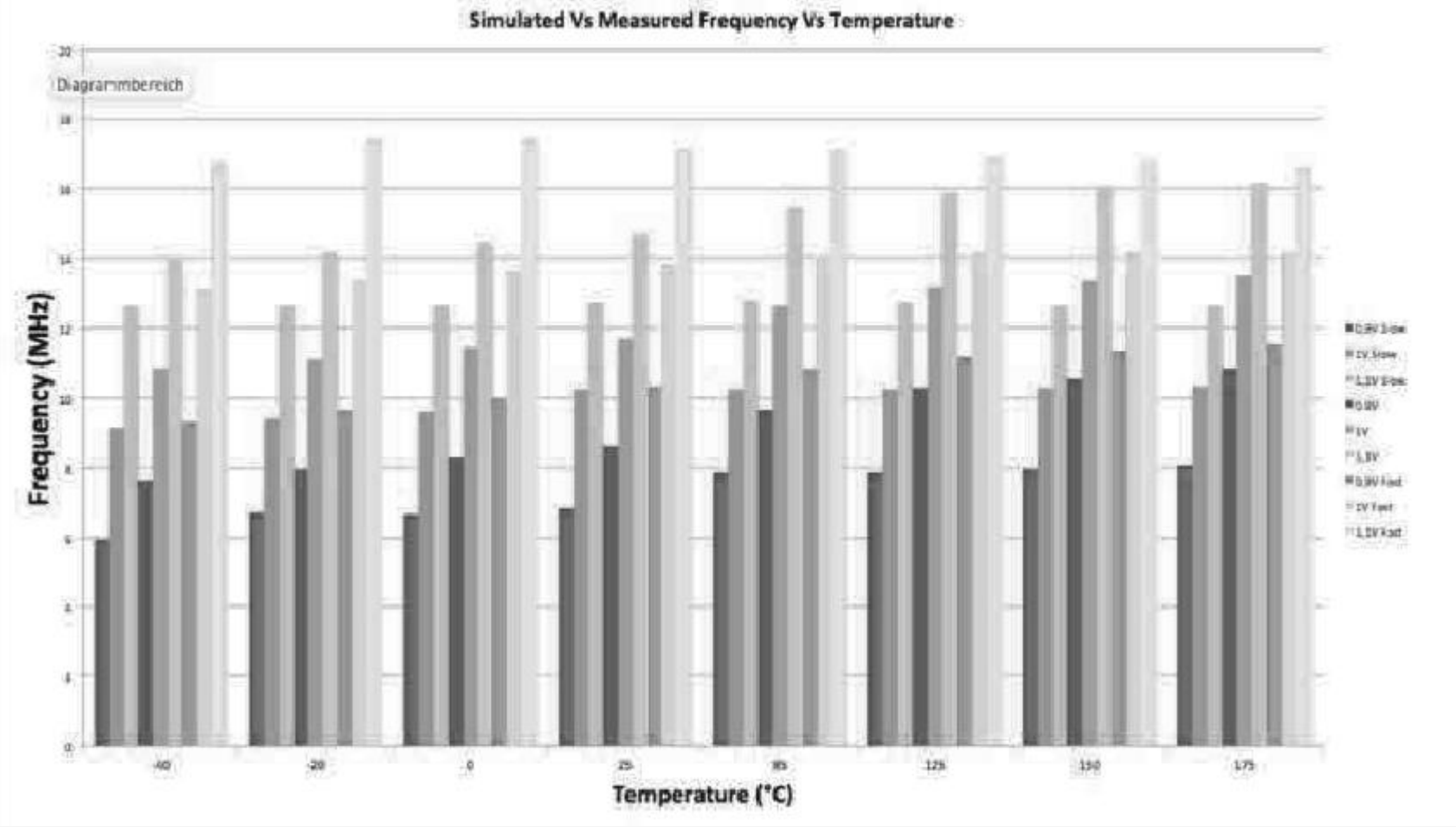
Electromigration, Reliability, Thermal Management are major concerns

Testchip28 Evaluation



Supply Sensitivity of 0.39%/mV

Testchip28 Evaluation



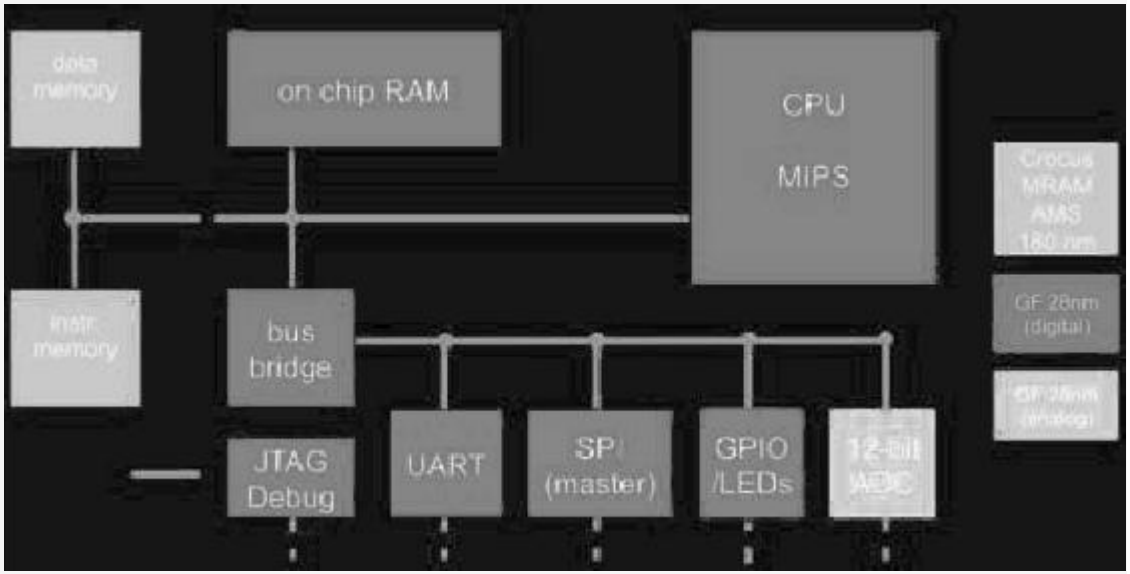
Red: Slow Corner; Blue: Measured Silicon; Green: Fast Corner

Testchip14

- Redesign of testchip28 logic sub-chip done for 14 nm technology
- Chip fabrication was not executed due to the high production costs of 14 nm technologies.
  It was not feasible within in ATHENIS_3D project budget and time frame.
- Evaluation was done in simulation versus the 28 nm design results
- As suggested as well by project officer and reviewers the LOGIC testchip sub-design was redesigned and simulated in GF 14 LP technology in comparison to re-simulation results for GF 28SLP sub-designs.
- Simulation result are comparable to 28 nm with even higher leakage, details to be found at the report
- A technology alternative has been found in cooperation with Globalfoundries:
  The new GF 22nm FDSOI technology, fabricated in Dresden, Germany.

SOC28 Overview

- Purpose: System on Chip for automotive applications at very high temperatures
- Imagination Technologies MIPS microAptive based microprocessor subsystem with DSP & FPU units
- Standard I/O, serial UART, SPI, I2C, GPIO interfaces
- 2 channel 12 bit ADC
- CPU debugging (JTAG)
- External MRAM interface (70 pins)

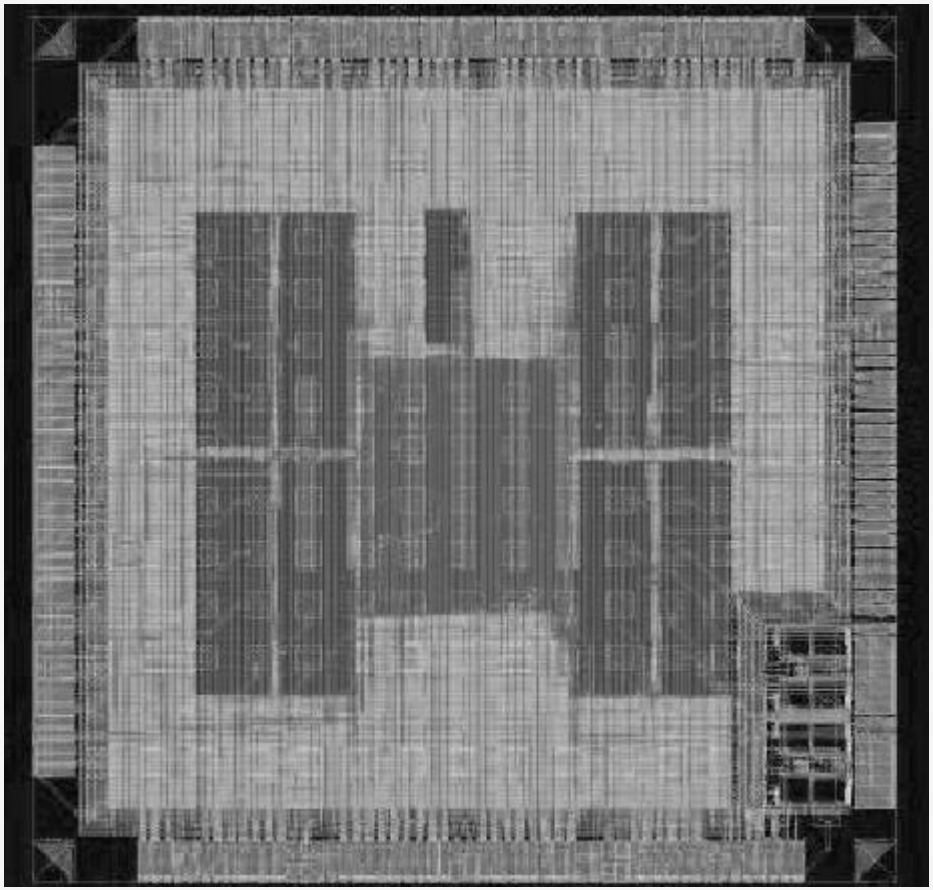


- Technology: GLOBALFOUNDRIES 28 SLP
- Complexity is 650k GE (gate equivalents)
- On Chip RAM (data and instruction), extended by ECC error correction. ECC error results are monitorable 32(56) bit x 16k
- 3D stackable with MRAM on interposer

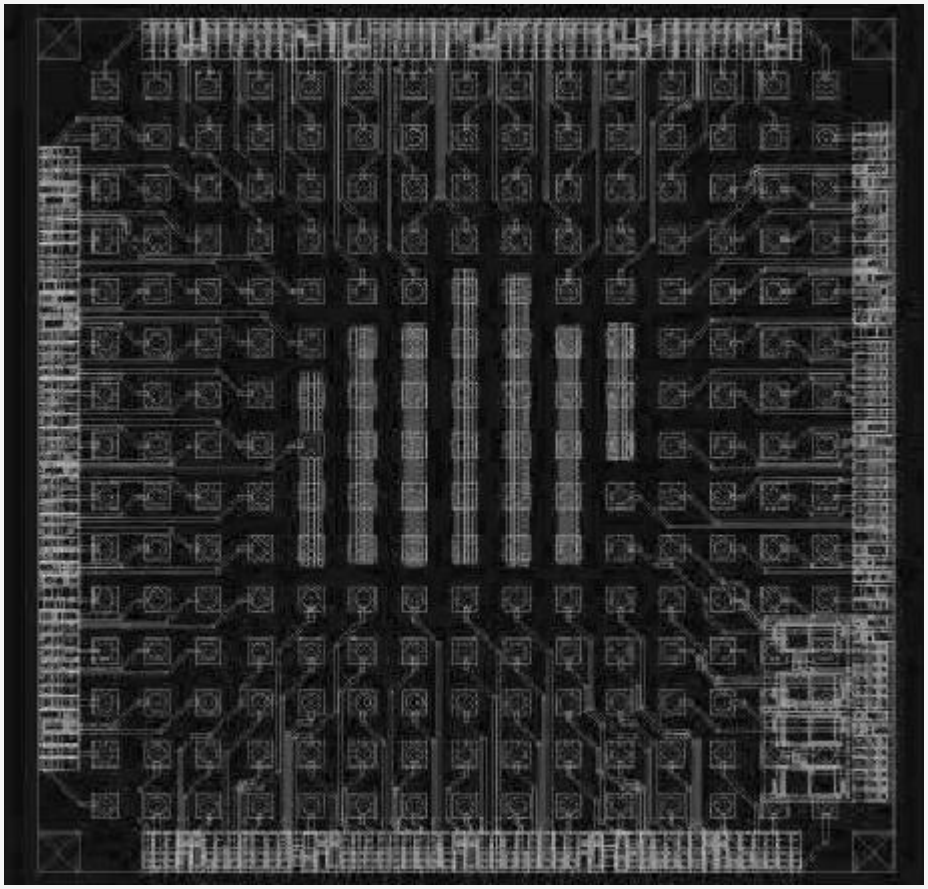
- In the design conservative methodologies as well as recommendations from GLOBALFOUDNRIES have been used to enable correct function at very high temperatures

SOC28 Layout

Chip layout

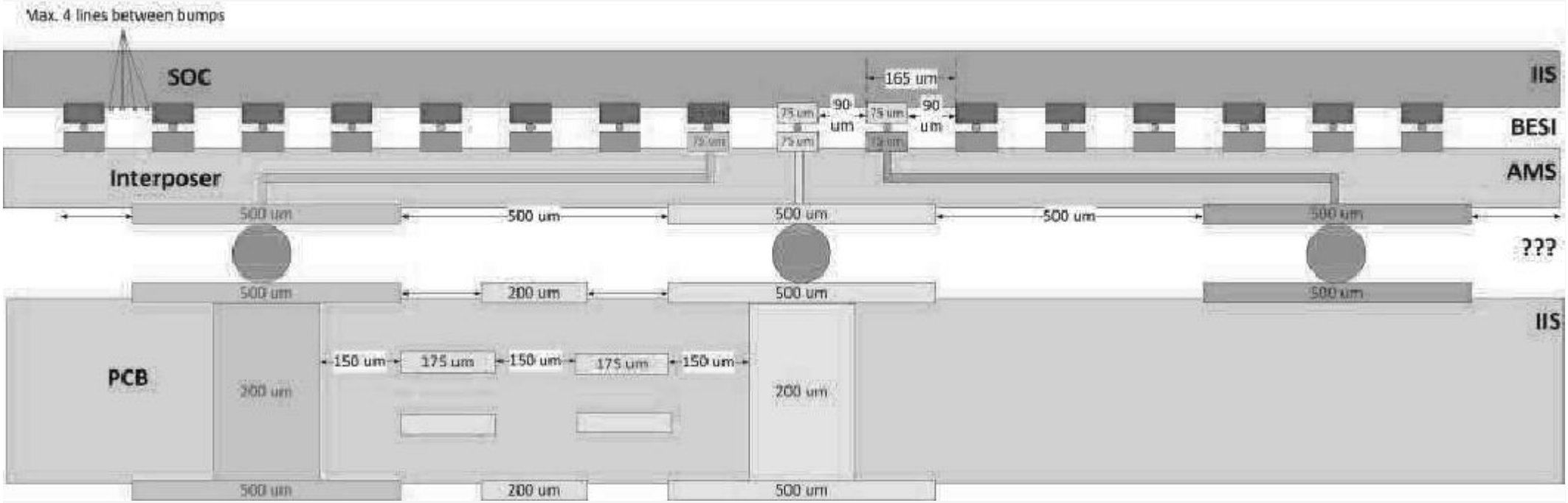


Redistribution Layer



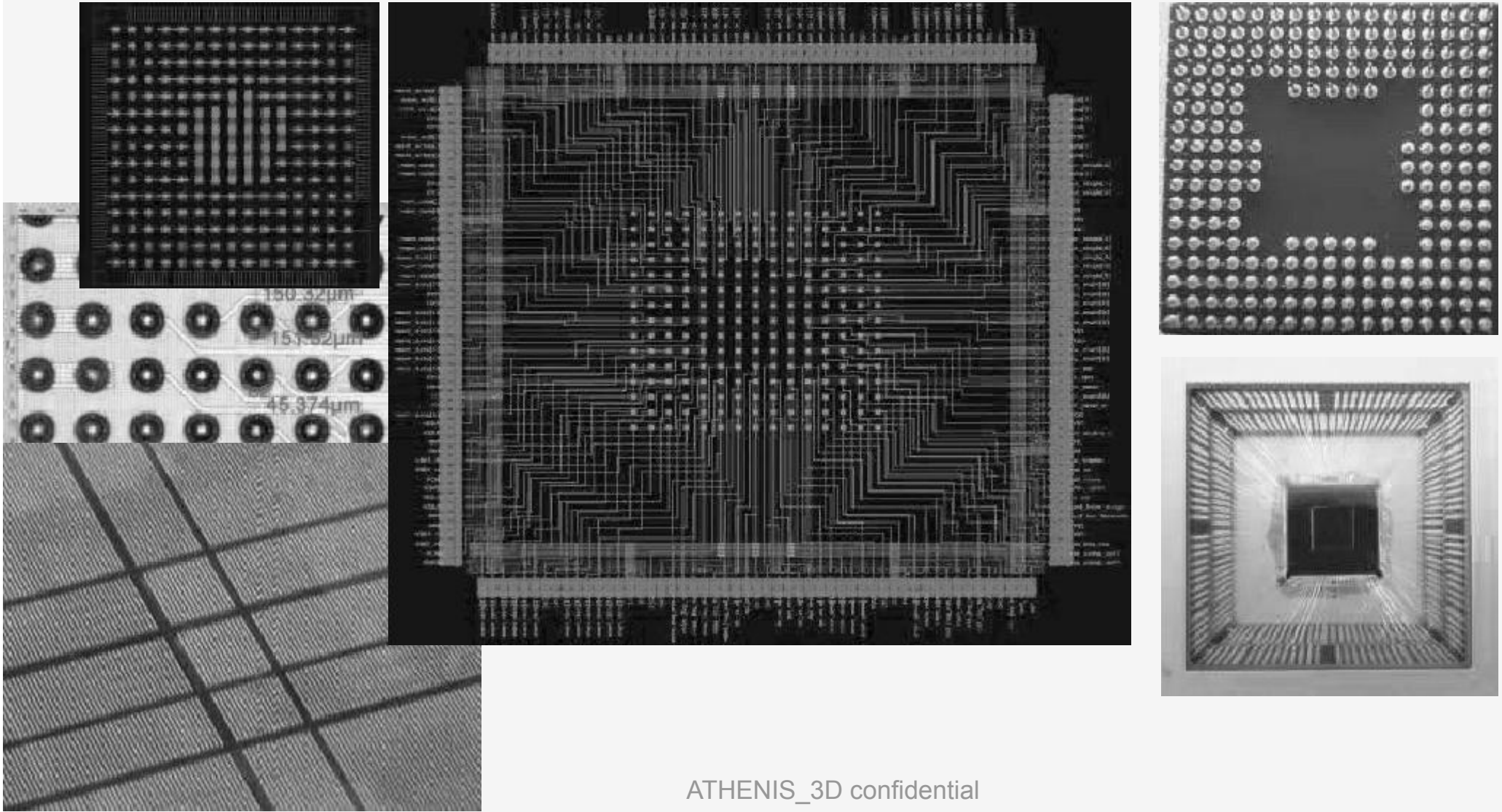
SOC28 Interposer

Original design with SOC28 and MRAM dies on interposer



SOC28 Flip Chip Mounting

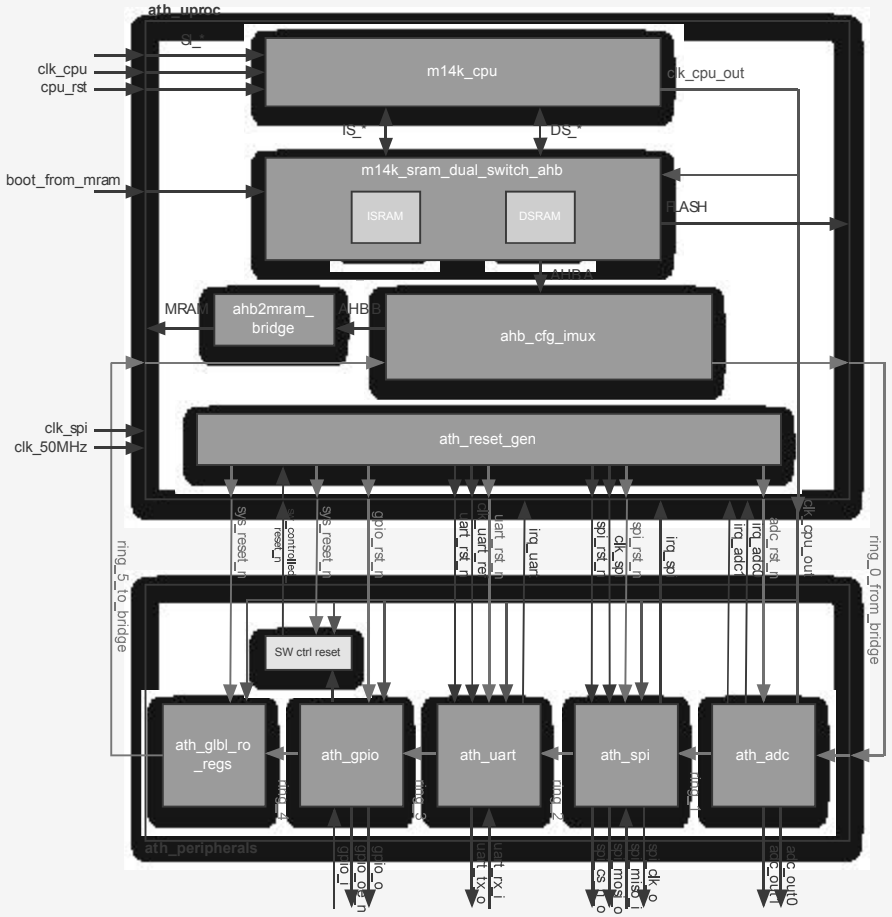
- Flip-Chip mounting on interposer bonded in PGA 225 package



SOC28 Evaluation

Running test programs verify:

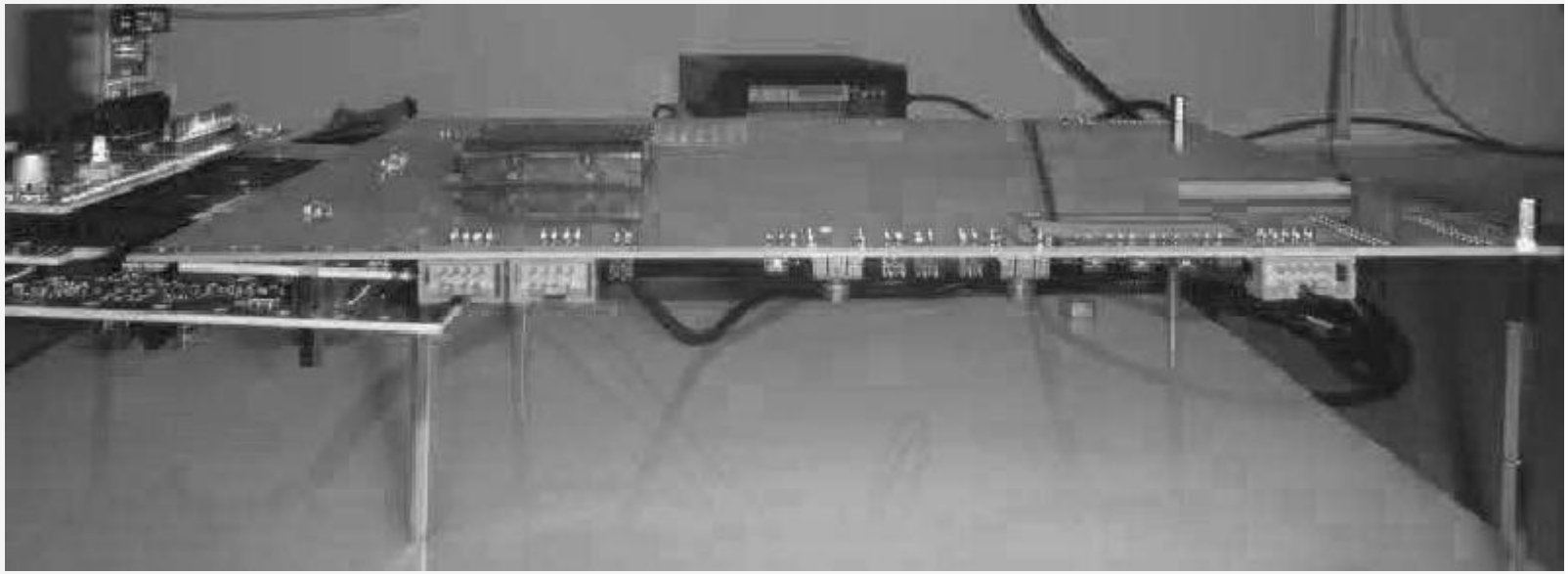
- CPU and Busses
- Instruction/data RAM
- Internal/external RAM/MRAM (emulated)
- Access to Interfaces
- Interfaces itself
- UART RX/TX
- GPIO Read/Write
- SPI Read/Write
- ADC Interface Access

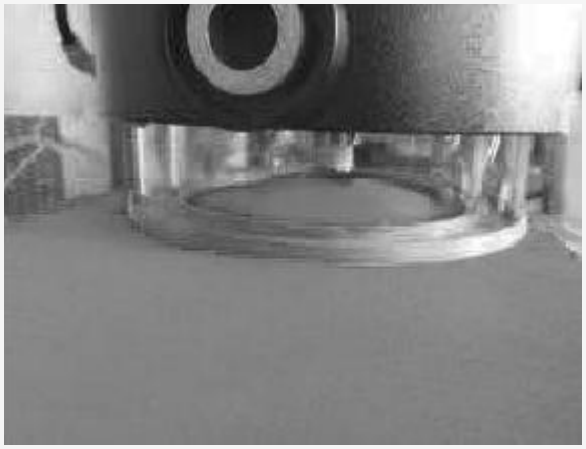


SOC28 Evaluation

Measurement setup with:

- FPGA controller board
- Dedicated testboard with SOC28





SOC28 Evaluation

- Frequency and temperature variation while evaluation
- 7 samples under detailed evaluation, further parts went to HTOL testing at Maser

Temperature	60 MHz	70 MHz	80 MHz	90 MHz	100 MHz	110 MHz	120 MHz
-40 °C							
-30 °C							
-20 °C							
170 °C							
180 °C							1
190 °C						1	3
200 °C				1	2	3	6
210 °C		1	2	2	4	5	7

Runs always
Runs always, but is not restartable/reloadable after fail at higher frequency
Runs never or fails during functional test

SOC28 Evaluation

- Functional tests after Packaging

Set	Samples	Functionally o.k.	Functionally partly defect, but usable for special tasks	Defect
1	5	1	-	4
2	5	4	1	-
3	57	49	7	1
Sum	67	54	8	5

- Functional tests after HTOL500 at 175°

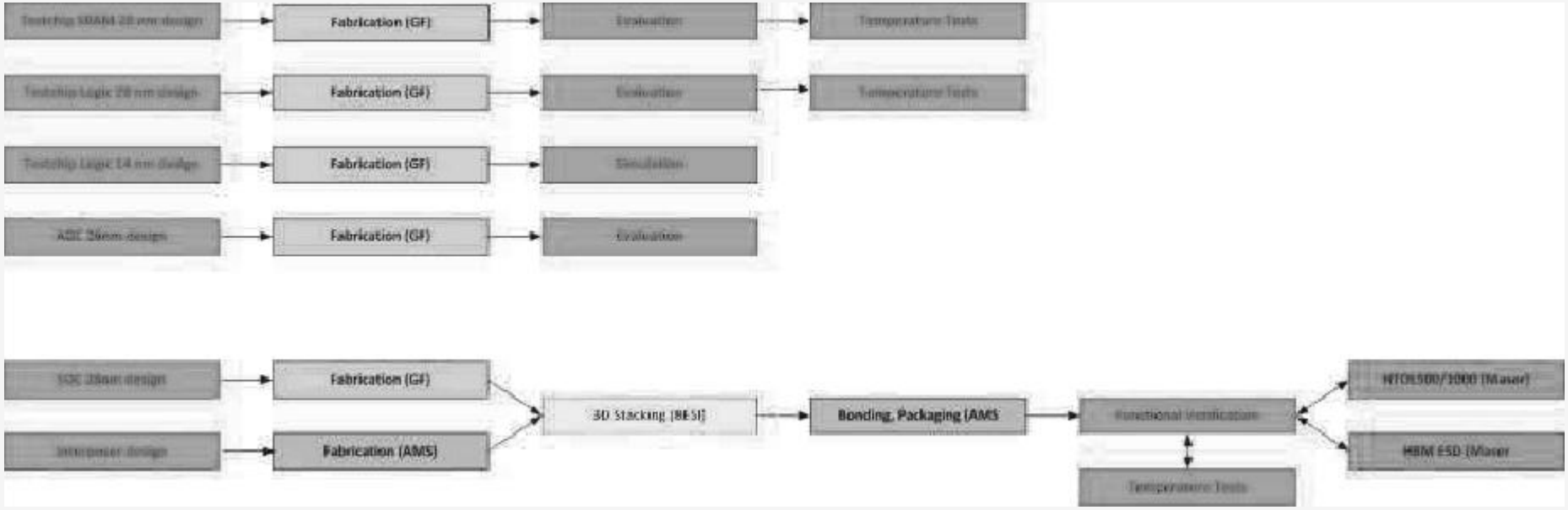
Set	Samples	Functionally o.k.	Functionally partly defect, but usable for special tasks	Defect
1	12	12	-	-

- Functional tests after additional HTOL500 at 200° C

Set	Samples	Functionally o.k.	Functionally partly defect, but usable for special tasks	Defect
1	12	12	-	-

(HTOLxxx: Hight Temperature Operating Life xxxh with 10 % higher Voltage)

Overview nano CMOS tasks with partner



Testchip22 FDSOI outlook

- GLOBALLFOUNDRIES 22FDX FDSOI technology has products architected to enable market segments from ultra lower power/low leakage to high performance and RF/Analog.
- Planar technology with an ultra thin silicon on buried insulator layer and transistors on top
- Fully Depleted means reduced random dopant
- Body/Back Gate Biasing Capability as an additional power/performance control
  - Reverse-Body-Basing (RBB) can be used to rise VT for RVT and HVT, Conventional Well (slower, low leakage)
  - Forward-Body-Basing (FBB) can be used to lower VT for LVT and SLVT Flipped Well (high performance, more power), close to FINFET-performance
- Cannot mix FBB and RBB in same logic Island
- New design methodology: From DVS (dynamic voltage and frequency scaling) to DBFS (dynamic biasing and frequency scaling)

Testchip22 FDSOI outlook

- Purpose is to quantify the effect of biasing at each VT level
- Two Testchips have been designed: RVT-HVT and LVT-SLVT
- A bias voltage generator (-2 V) and a dynamic bias controller IP have been designed
- Tapeout was done end of March 2017 (Results not within ATHENIS_3D project)
- Samples expected beginning July 2017
- Evaluation is planned to cover high temperature tests similar to ATHENIS_3D