WP5: TEST CHIP DEVELOPMENT

Leader:	**Università di Pisa (UNIPI) – Sergio Saponara**
Start:	M7
End:	M40

WP5 Planned effort and Deliverables

Planned Efforts

Work package		AMS	VEEM	Crocus	FHG	TUW	UNIFE	AT	MASER	BESI	CEA	UNIPI	Total
WP5	Planned person.months per participant	16,5	12,5		43,0				0,0		3,0	33,0	108,0

Deliverables

D5.1: M27 ✓ Report on Testchip design [AMS]
D5.2: M36 ✓ Design, fabrication and characterization of circuit blocks [AMS]
D5.3: M37 ✓ ESD and EMC chip characterization [AMS]
D5.4: M40 ✓ Testchip characterization at high temperatures [MASER]
D5.5: M40 ✓ Design, fabrication and characterization of controller circuit on 28nm/14nm node [FHG]

Milestone

MS5 M27 ✓ Design of testchips (demonstrator 1&2) completed

WP5 Actual effort and Deliverables

Actual Effort

Work package		AMS	VEEM	Crocus	FHG	TUW	UNIFE	AT	MASER	BESI	CEA	UNIPI	Total
WP5	Planned person.months per participant	17,2	12,5		83,4				2,1		1,0	45,6	161,8

Tasks

T5.1 Design of Demonstrator Prototype [AMS]
T5.2 Design of DCDC converter using IPDs [UNIPI]
T5.3 Advanced control techniques for 48V DCDC using IPDs [UNIPI]
T5.4 Design, production and evaluation of controller circuit in 28nm/14nm CMOS [FHG]

- **In WP5 Milestones Completed**
- **In WP5 Deliverables Completed**
- **From WP 5 activities 1 patent has been generated (VALEO/UNIPI)**
- **From WP 5 activities 12 publications have been published, 2 submitted (UNIPI, VALEO, AMS)**

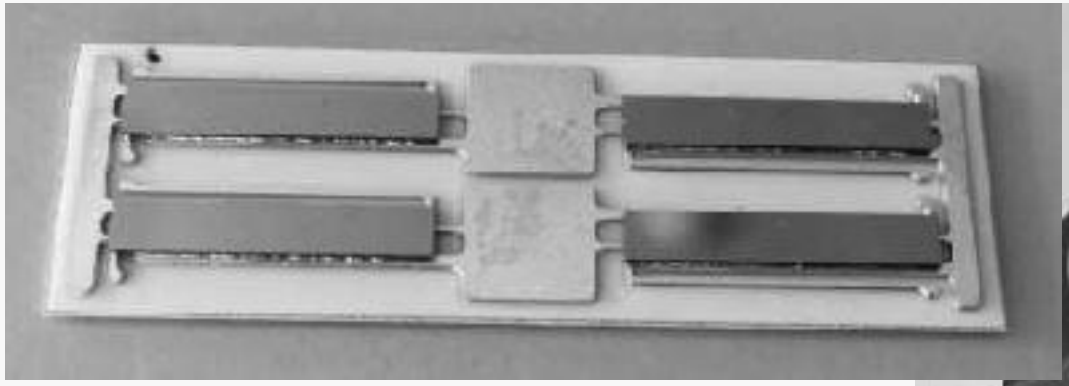
WP5: T5.1 Design of Demonstrator Prototype

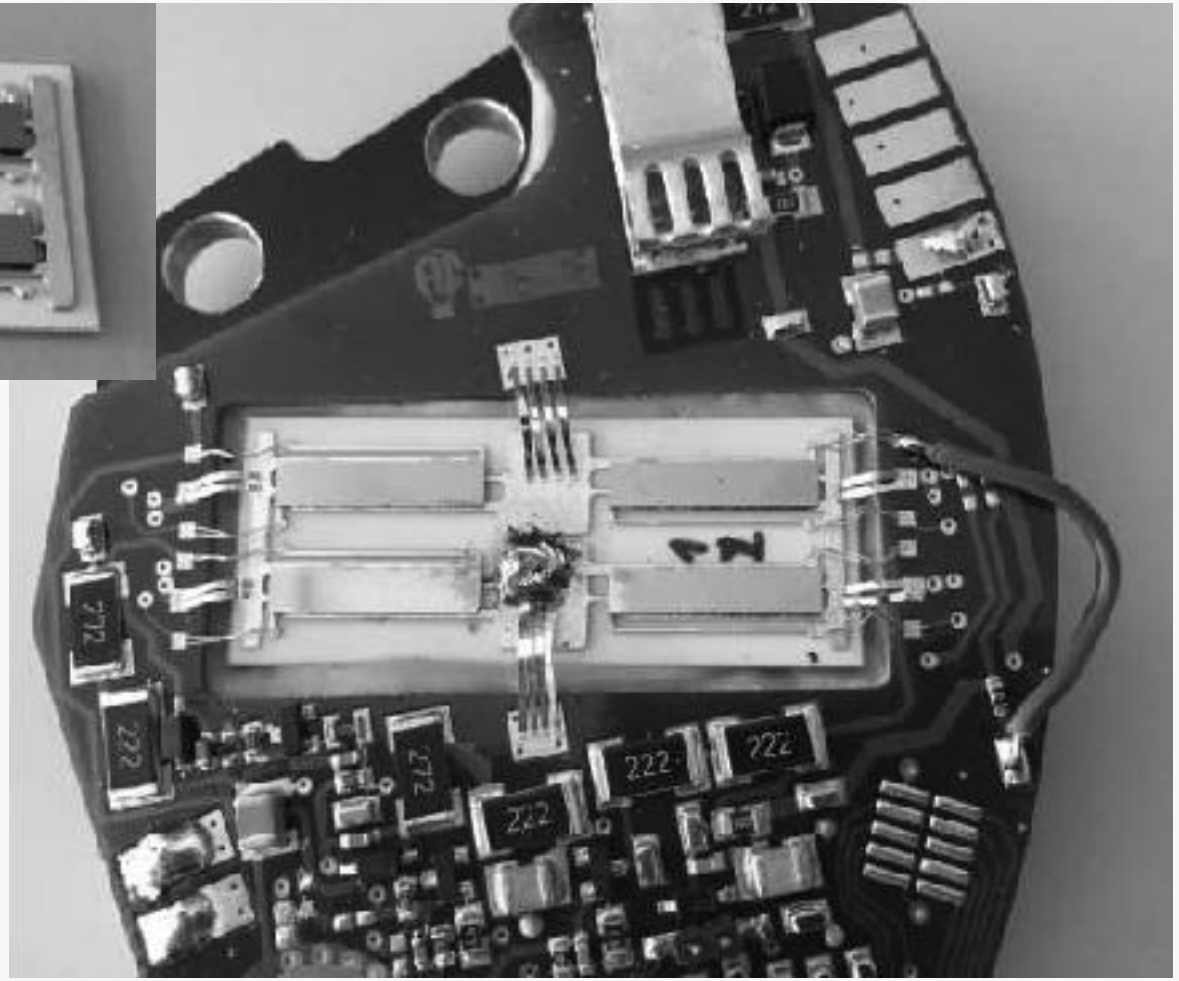
Achievements / Challenges

- 3D integrated H-bridge demonstrator (transistors and DBC) has been defined iteratively in close interaction with Valeo and DBC supplier
- H-bridge transistor design and layout has been validated by simulation of interconnect resistance and required tightened DBC specs
- H-bridge transistor including UBM/balling, DBC manufacturing and D2W successfully manufacted
- Evaluation showed >5x reduction of Ron with new 3D integration approach and further Ron reduction capability due to parallelization concept
- ESD characterization showed weakness of PMOS ESD protection but with >1kV with ESD safe handling procedure assembly of samples was possible
- Characterization up to 200ºC showed expected behaviour and technology robustness
- H-bridge demonstrator in demo car realized and validated with a discrete control concept from Valeo

WP5: T5.1 H-bridge

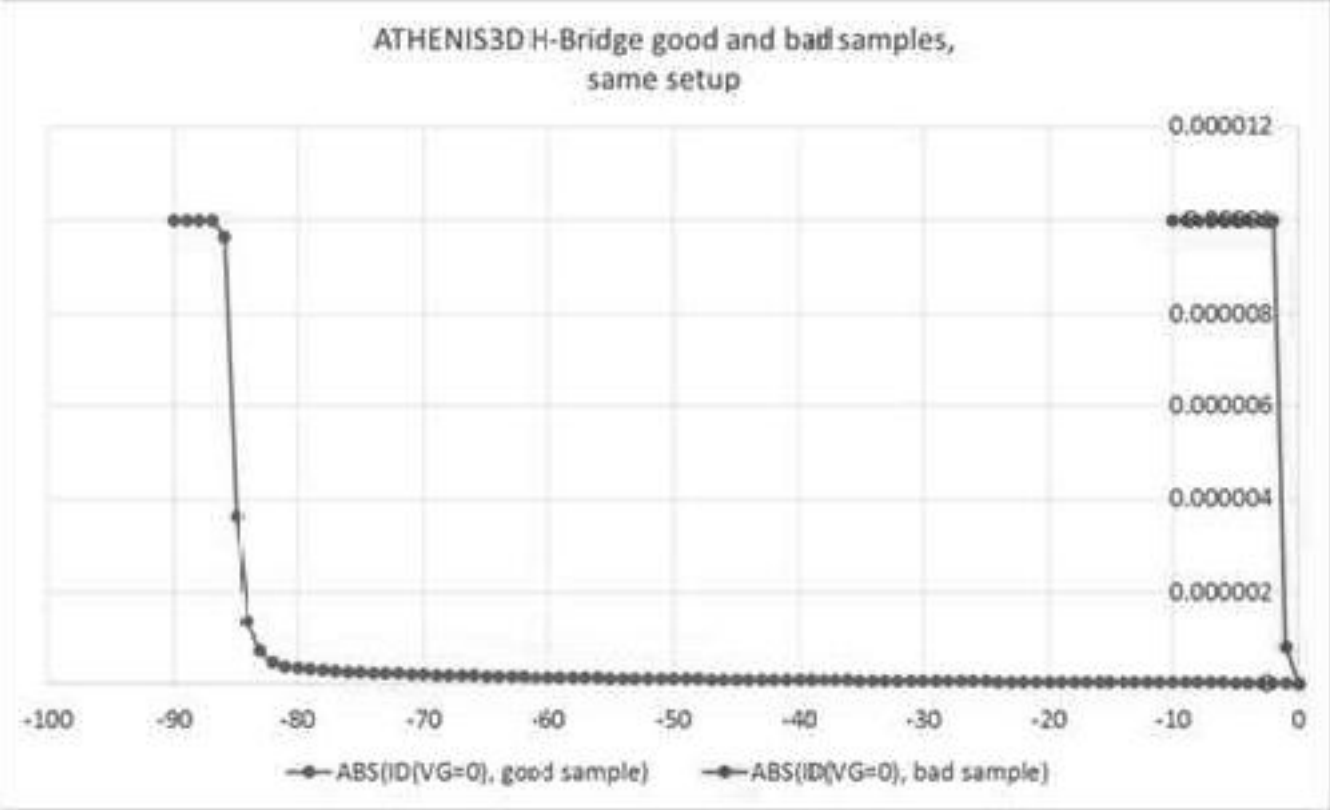
H-bridge consisting of 4 transistors (2x NMOS, 2x PMOS) stacked on DBC board





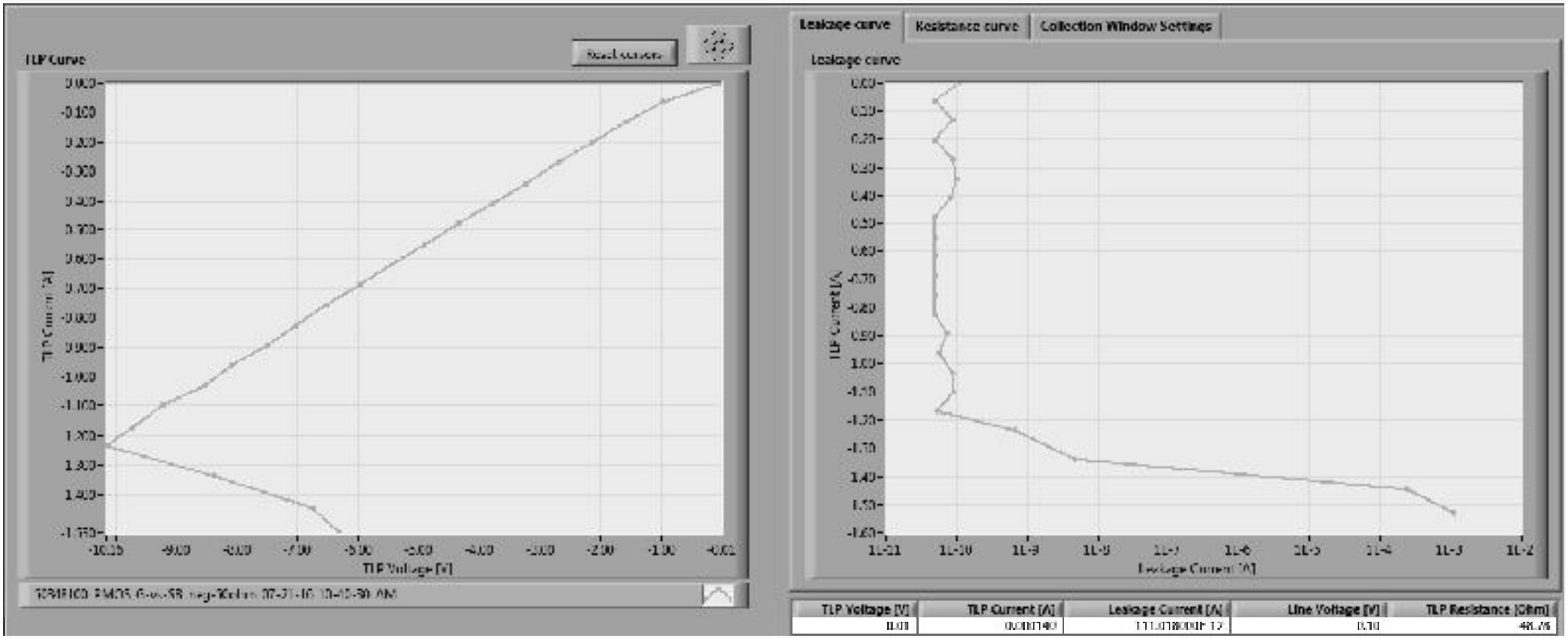
WP5: T5.1 H-bridge failures

- Sample returned from Valeo for FA: leakage on transistor T1 PMOS
- Short @ PMOS verified



WP5: T5.1 H-bridge – ESD

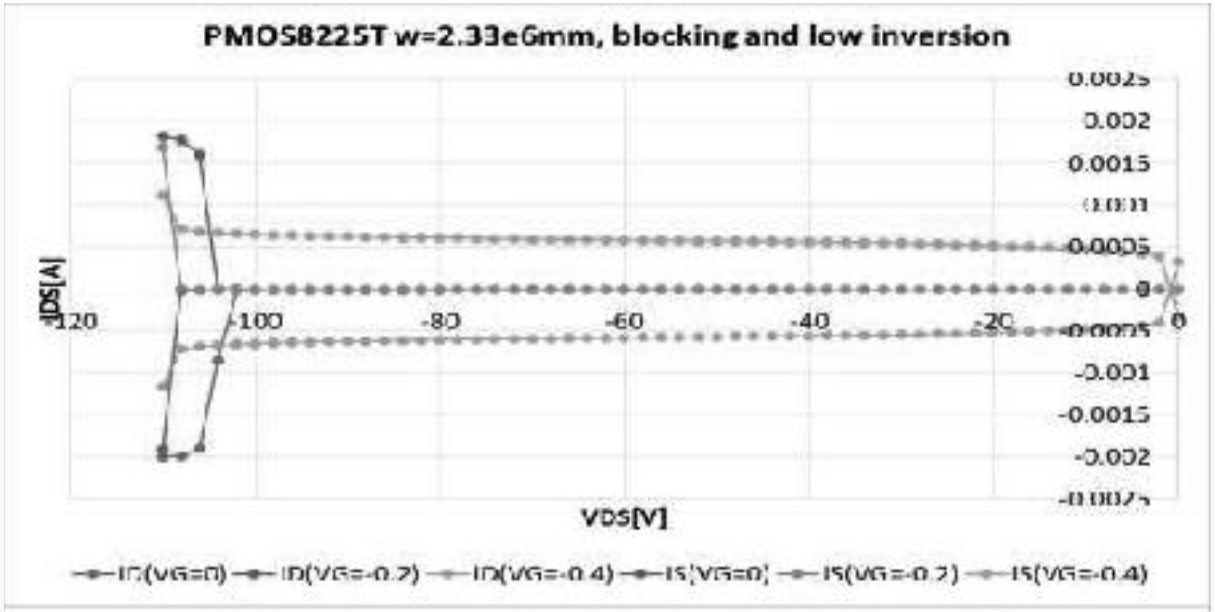
- ESD tests showed that gate protection of PMOS is only 1kV (up to 1.5kV)
  not ESD safe handling can destroy PMOS and lead to leakage
  => instruction for ESD safe handling to all partners

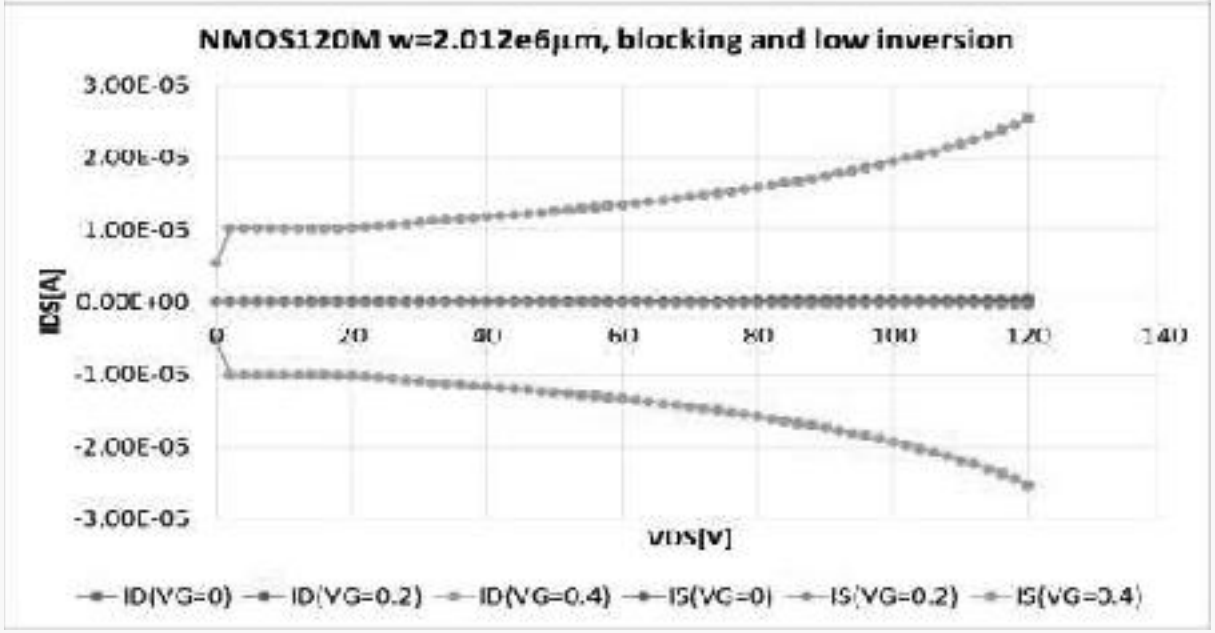


ATHENIS_3D confidential

WP5: T5.1 H-bridge BV

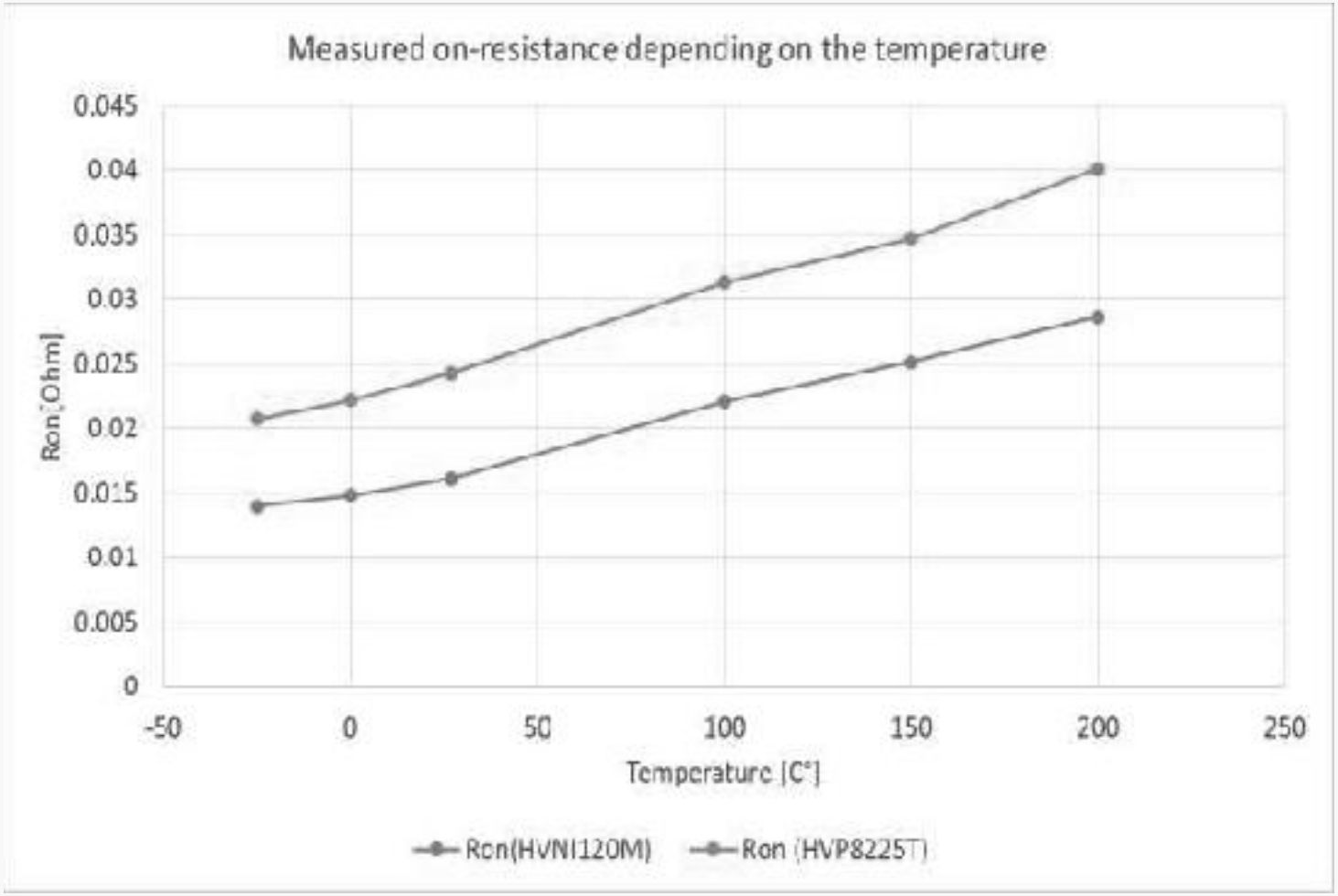
Voltage blocking
NMOS and PMOS





WP5: T5.1 H-bridge Ron

Ron of HV-NMOS and HV-PMOS over temperature



WP5: Task 5.1 H-bridge controller

Status

- Instead of the full H-bridge driver design to be performed by CEA LETI AMS and Valeo have agreed to subcontract the development of a concept and schematic for the MOSFET driver to **UPMC** Université Pierre et Marie CURIE.

- This includes
    - slew rate control di/dt control for high-side MOS switching,
    - temperature and
    - current measurements of the power MOS and
    - reverse polarity breakdown protection.

- Same PMOS layout selected as validated in H-bridge

WP5: Task 5.1 H-bridge controller

Achievements / Challenges

- 3 party NDA finished (ams, UPMC, Valeo)
- Cooperation contract finished (ams, UPMC)
- ams design kit installed @ UPMC
- Description of transistor and H-bridge concept provided
- Layout of PMOS and NMOS H-bridge driver transistors provided
- Models for NMOSI120M and PMOSVS8225T (design kit patch-update) provided
- Updated Spec documentation from Valeo provided
- The study investigated state-of-the-art for the H-Bridge current control during switching
- New gate driver concept and model development and reviewed iteratively
- Power loss and EMC characteristic were optimization parameters
- EMC turned out to be the most critical issue, as different switching frequencies and gate current pulse shapes can negatively influence the EMC characteristic

- Concept and model developed for high side switch control, final layout needs thorough consideration of integration and related parasitics to provide low EMI

High Side Driver

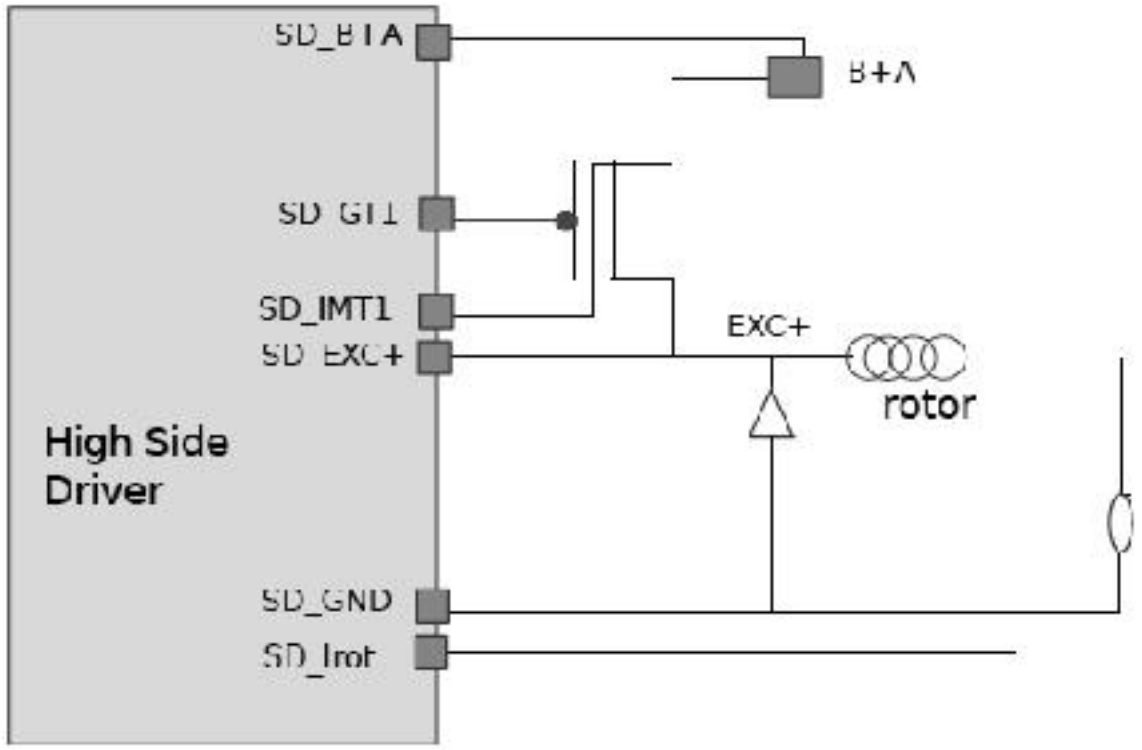
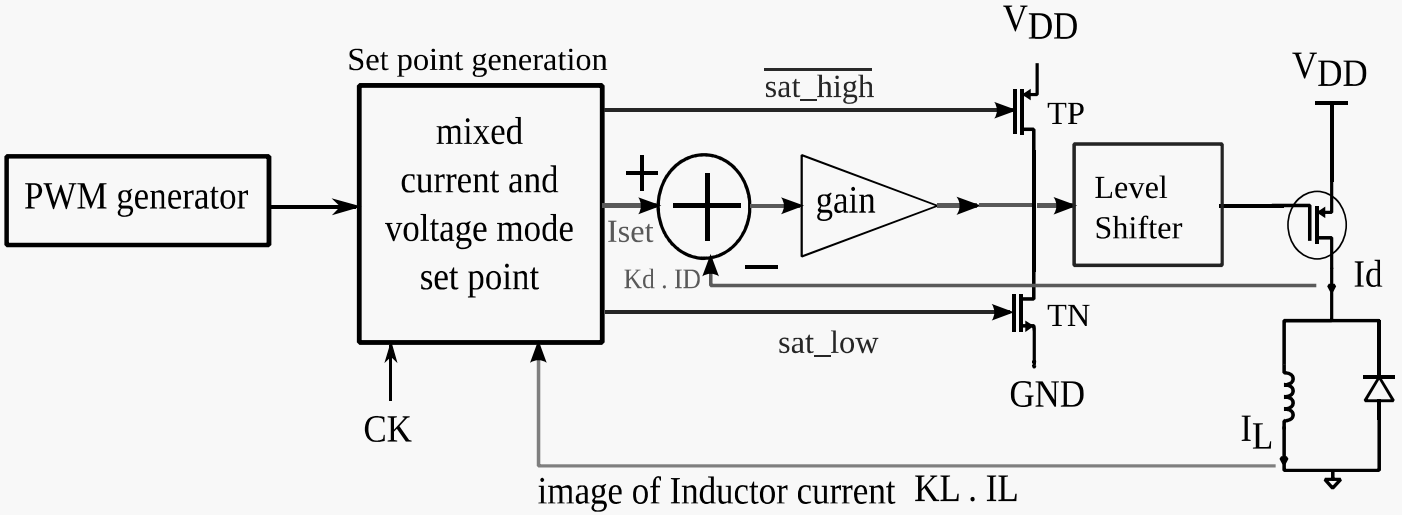


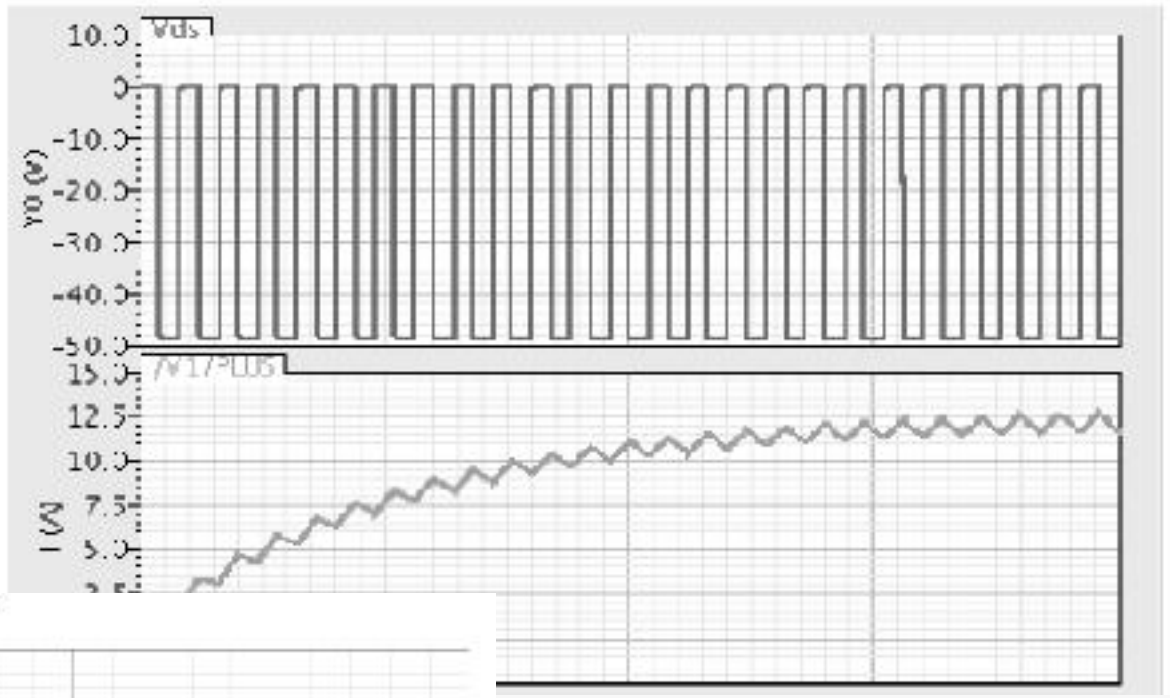
Figure 1 : High Side Driver

Driver Control Concept



WP5: H-bridge driver

Driver Control Concept



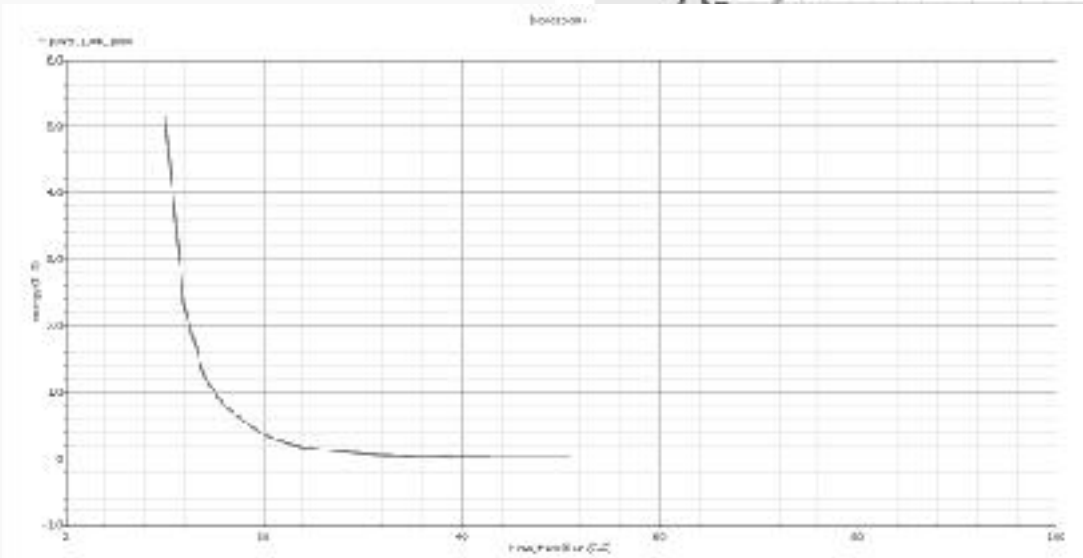
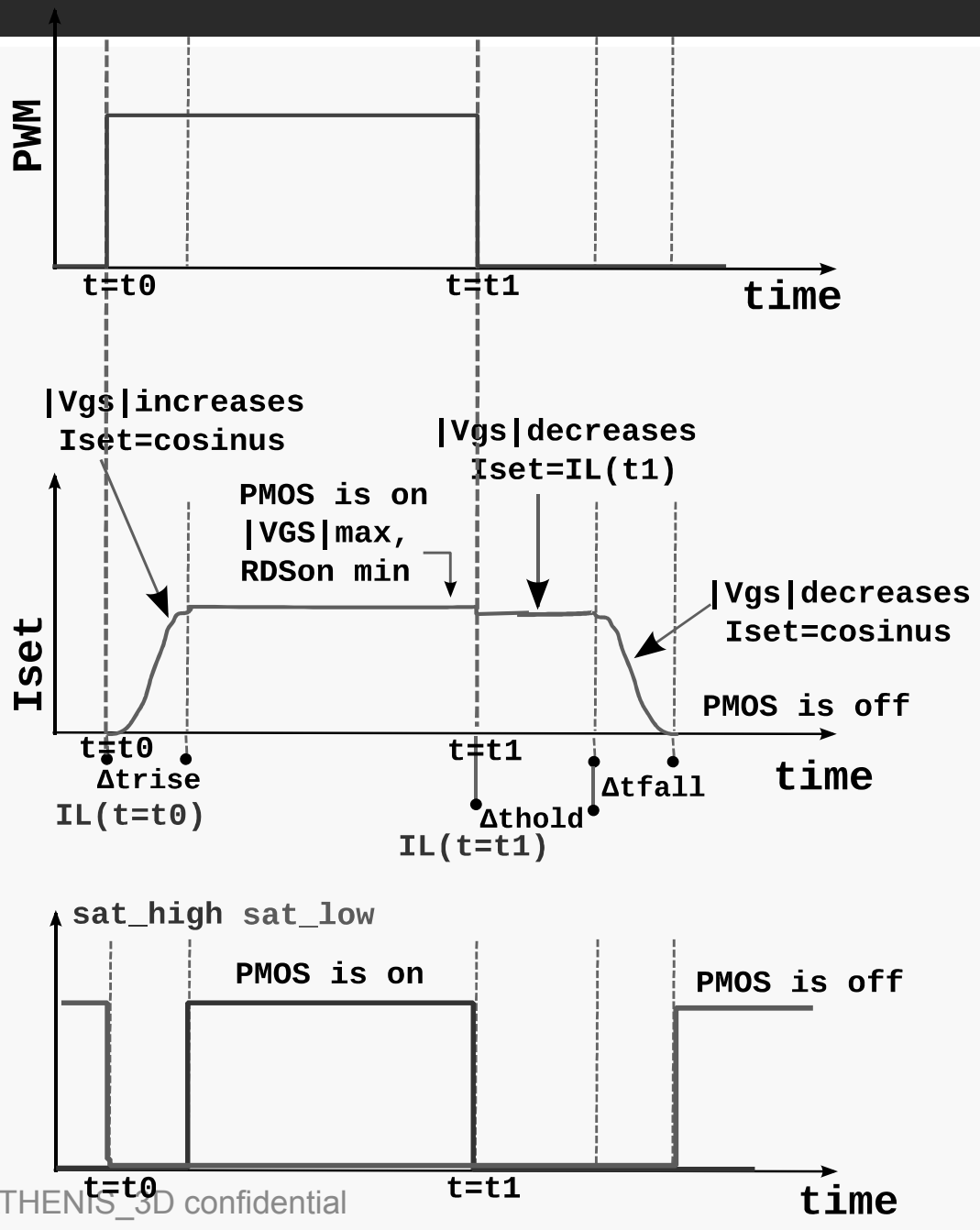


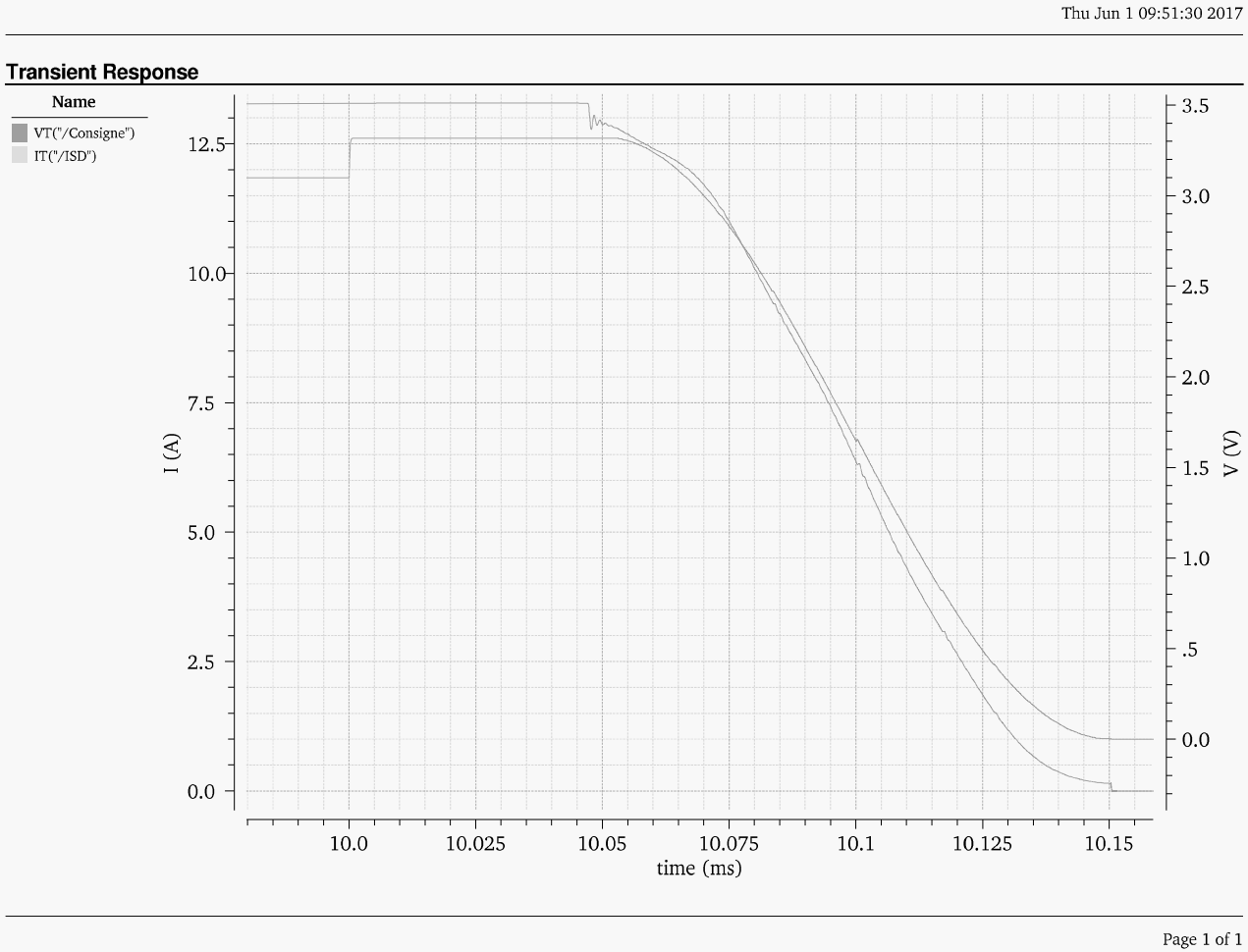
Figure 6: Power spectrum of the PMOS drain current (between 100 KHz and 1000 MHz), function the rising time going from 10us to 100us.

High Side Driver

Further control steps introduced to control transition steps



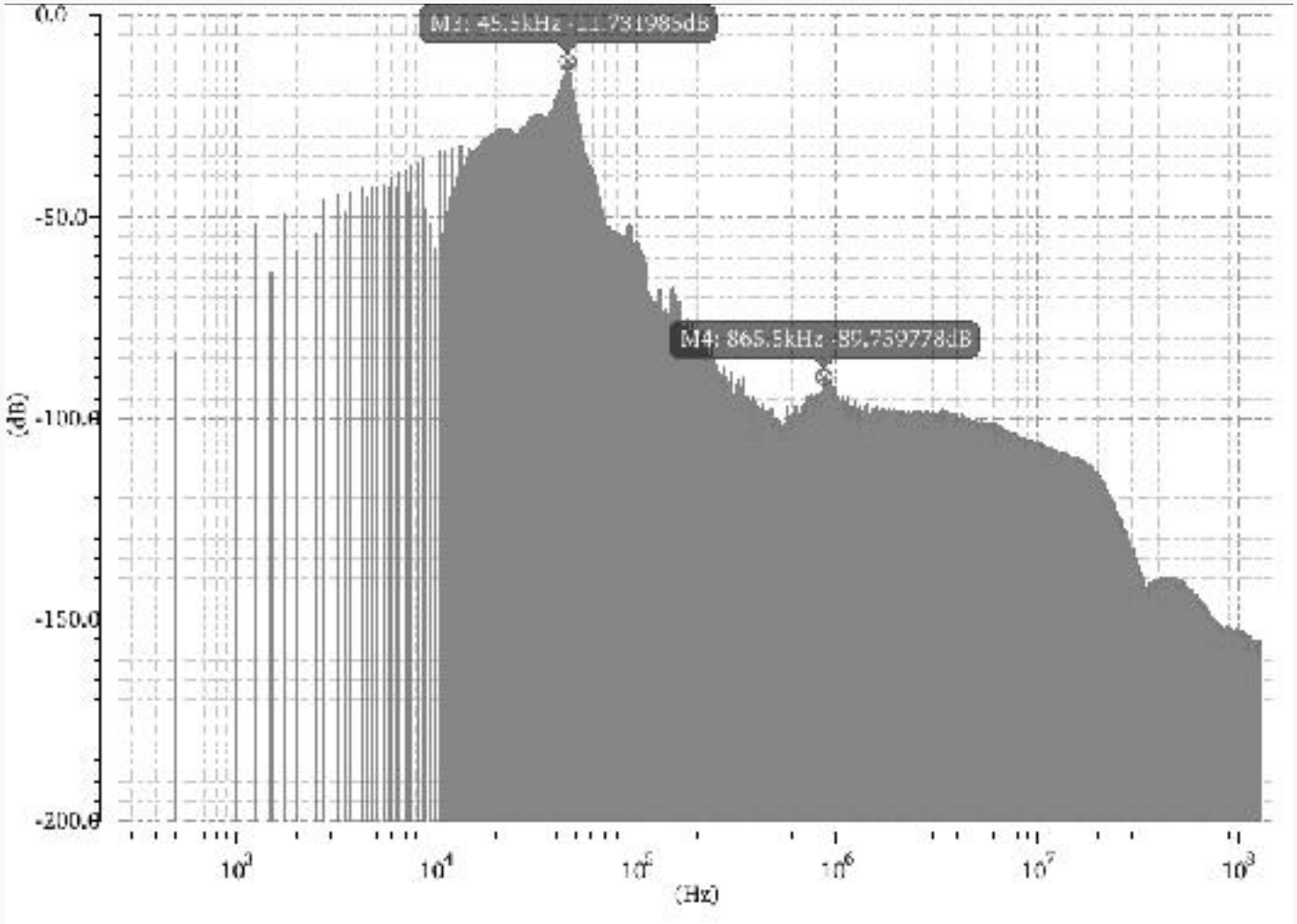
High Side Driver



Timing diagrams of current setpoint (“consigne” in green) and PMOS transistor drain current in blue, during falling phase, when the slope is set to 0.125 A/µs.

WP5: H-bridge driver

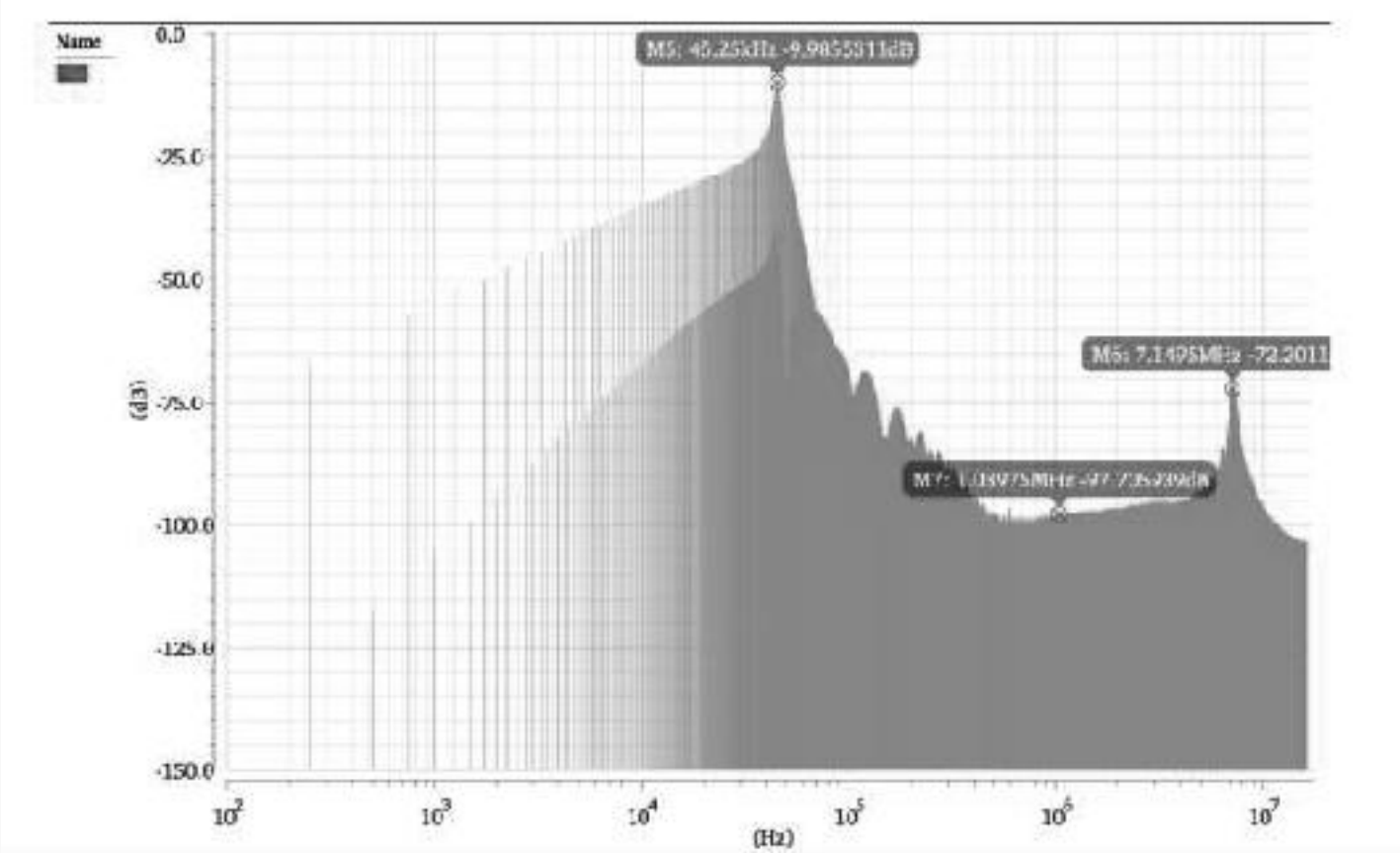
PMOS EMI spectrum



Spectrum of the measurement voltage using EMI evaluation circuit when the rising and falling slopes equal 0.625 A/µs

WP5: H-bridge driver

PMOS EMI spectrum – further enhancements demostrated



Spectrum of the measurement voltage using the EMI evaluation circuit when the rising and falling slopes equal 0.625 A/µs and the ideal current source shows 2 steps

T5.2: Design of DCDC converter using IPDs [Leader: UNIPI]

Start: M7

End: M36

Objectives:

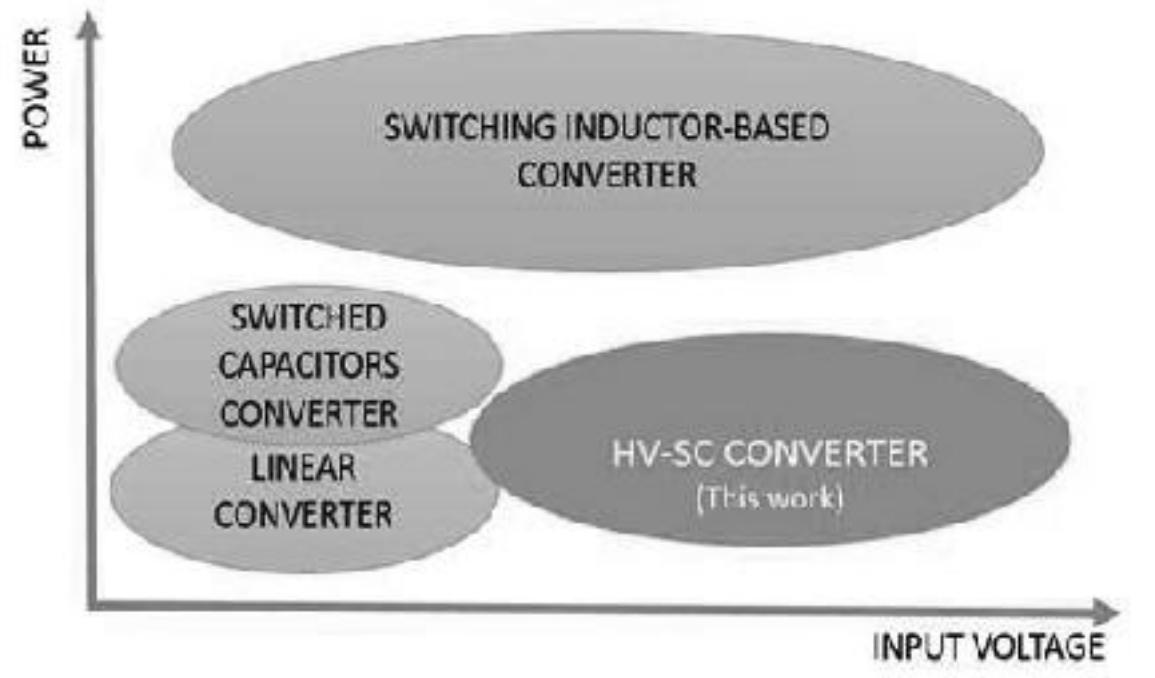
O5.2: Develop the testchip for the 48 V DCDC converter (demonstrator 2)

Status

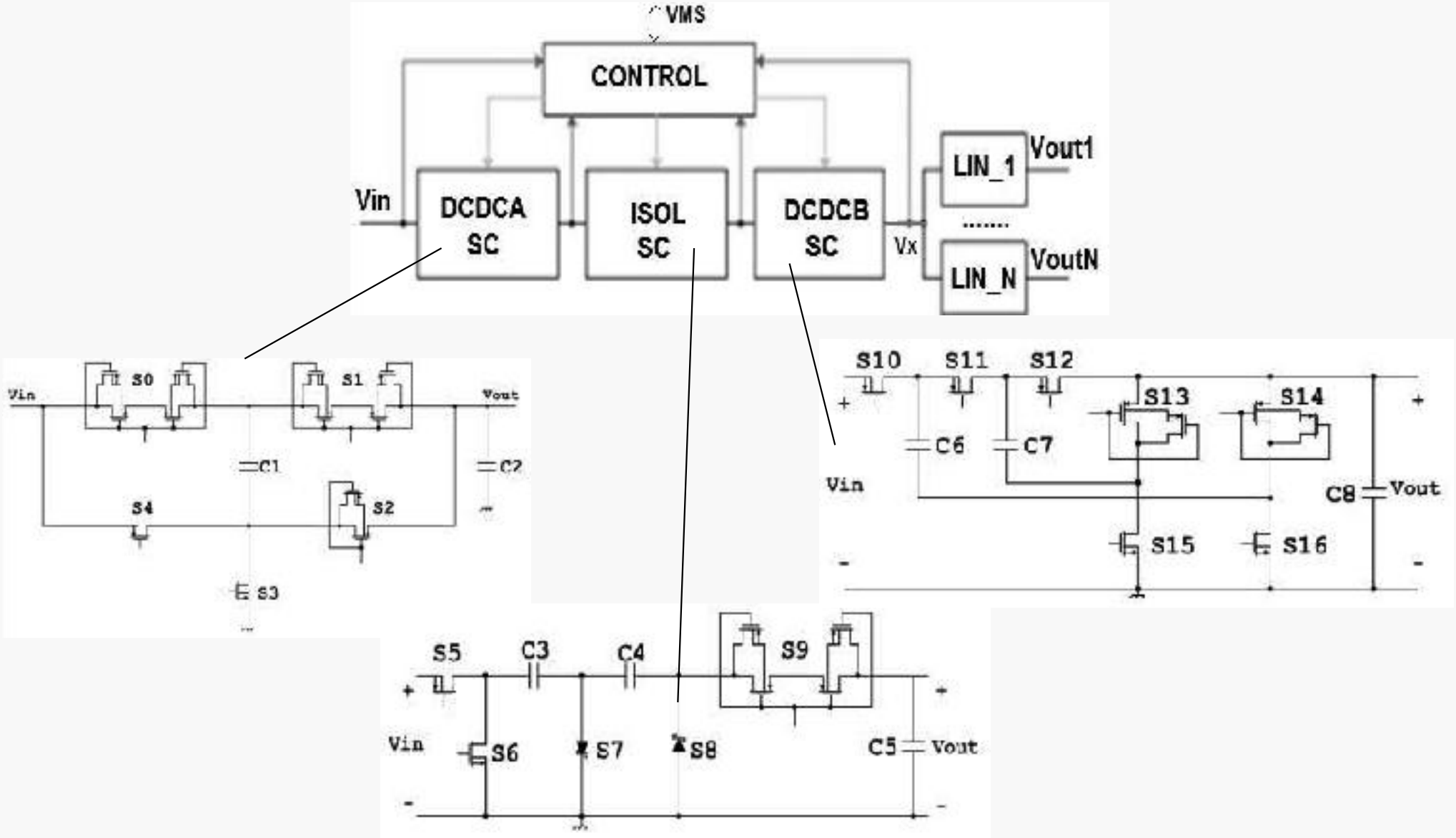
- 3 different ICs (inductorless DC/DC converter) have been designed and tested in terms of EMI, ESD, thermal and electrical (PSRR, line and load regulation, efficiency, ripple)
- **V1:** The DCDC converter has to convert the 48V battery voltage (ranging from few V to 60 V) into 24V (single-stage switched capacitor IC architecture). Conversion from 48 V to 12 V through a dual stage implementation. Chip available in DIL ceramic package. Digital control outside the chip implemented through a microcontroller
- **V2:** The DCDC converter has to convert the 48V battery voltage (ranging from few V to 60 V) into 5V and 1.65 V output loads (multi-stage switched capacitor IC architecture with patented isolation stage). Digital control integrated inside the chip. Chip available in DIL ceramic package or as naked chip directly bonded on the testing board.
- **V3:** Same as V2 but with capacitors stacked on top of the naked chip through an interposer

The proposed DC/DC converter covers a gap in state of art (switched cap inductorless converter for high voltage input and low power loads)

e.g. supplying processors, memories, sensors starting from 12V, 14V or 48V battery systems in hybrid/electric vehicles or also in telecom systems

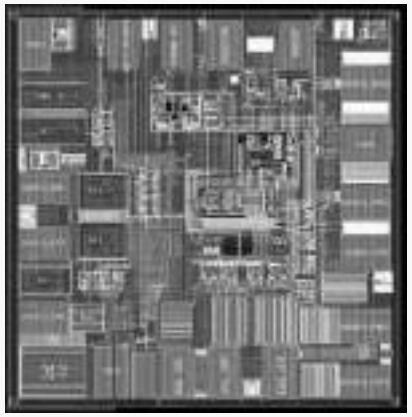


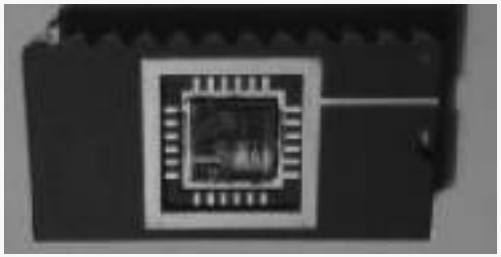
WP5: Inductorless architecture



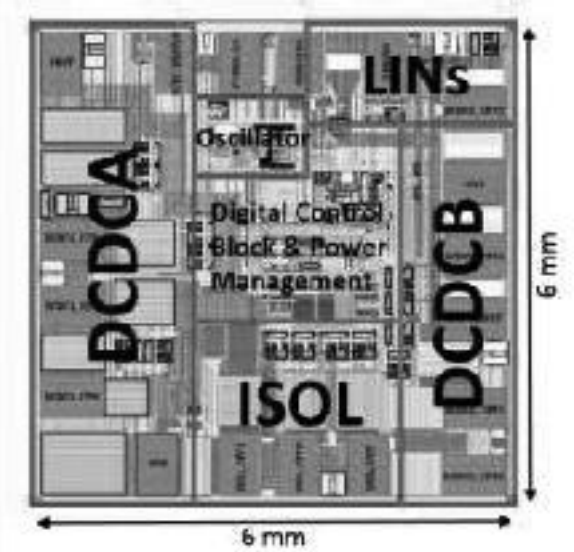
WP5: V1 & V2 chip layout and test PCB

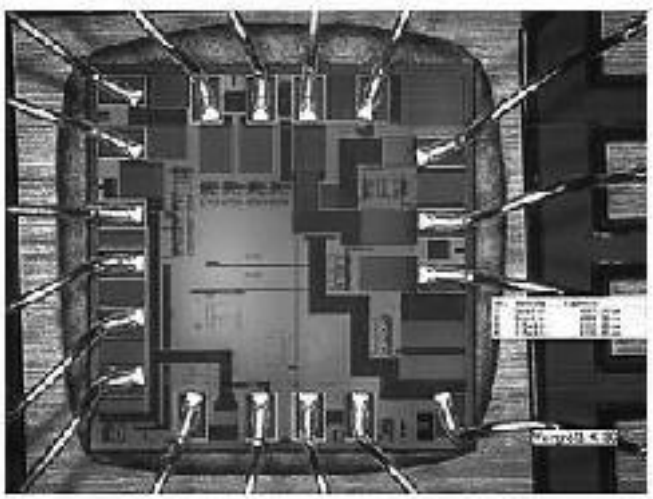
V1

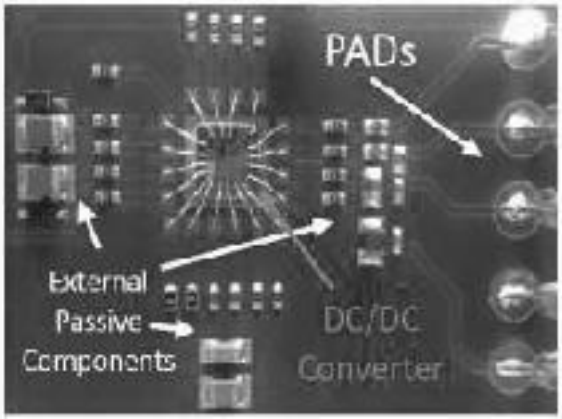




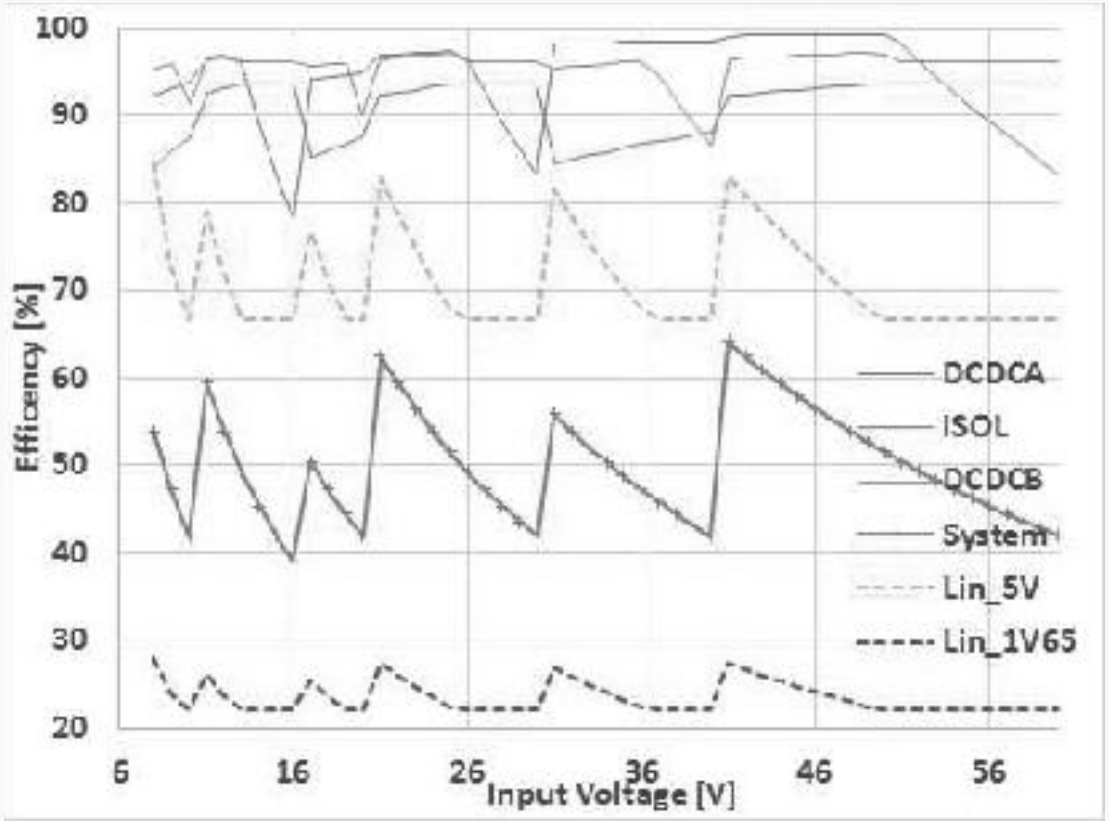
V2



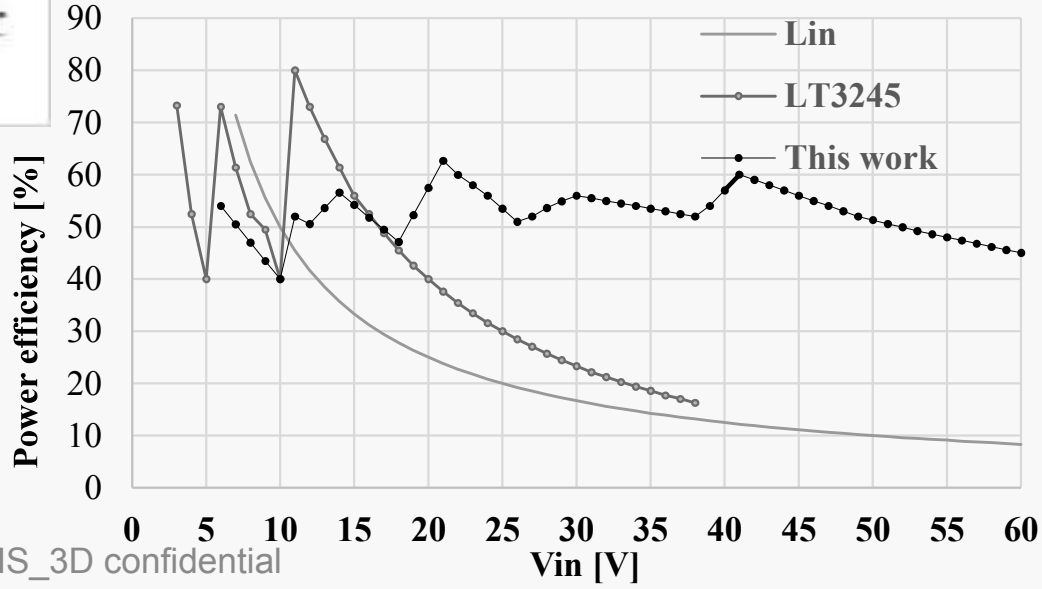




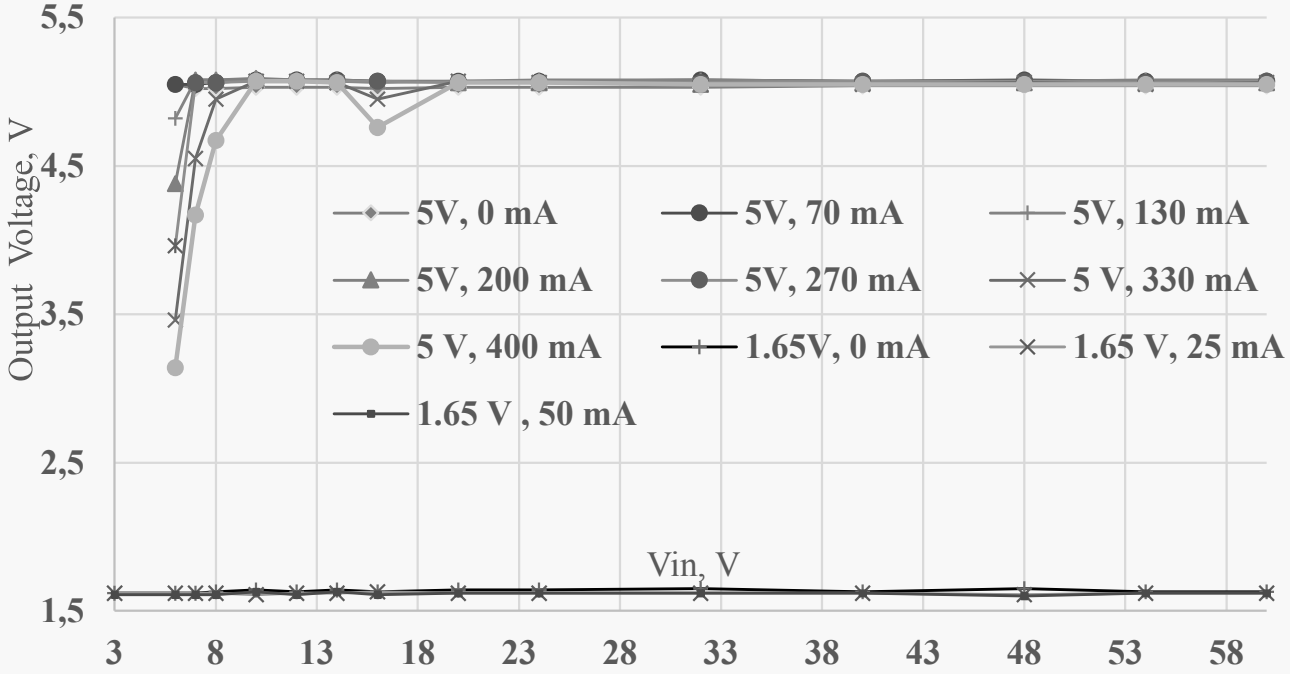
WP5: V2 efficiency measurements



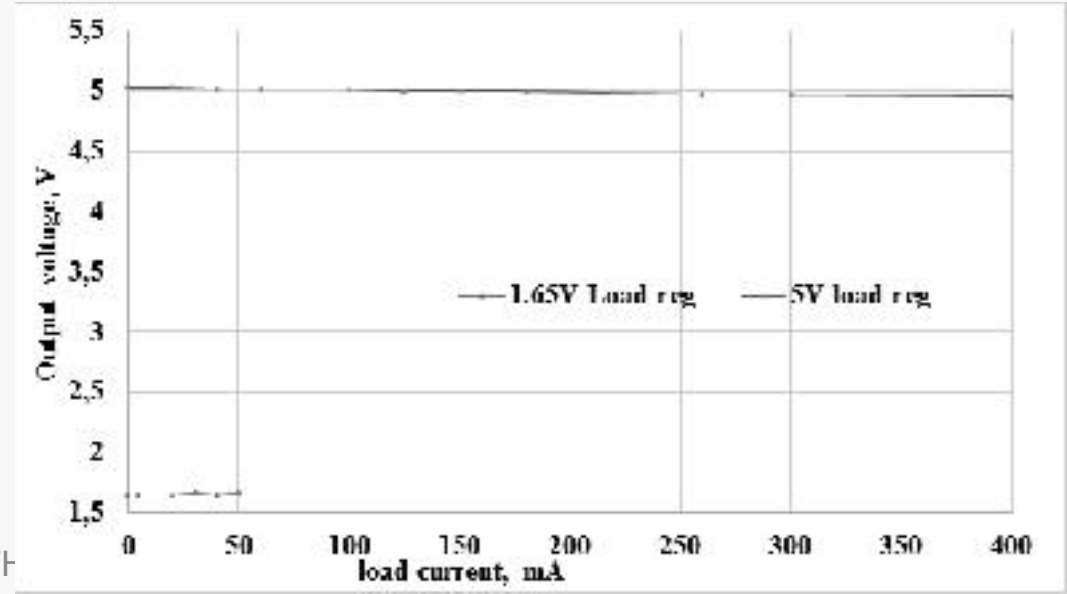
Efficiency of 50-60% much better than linear regulators and than competing ICs in a wider input range (suited for low power loads)



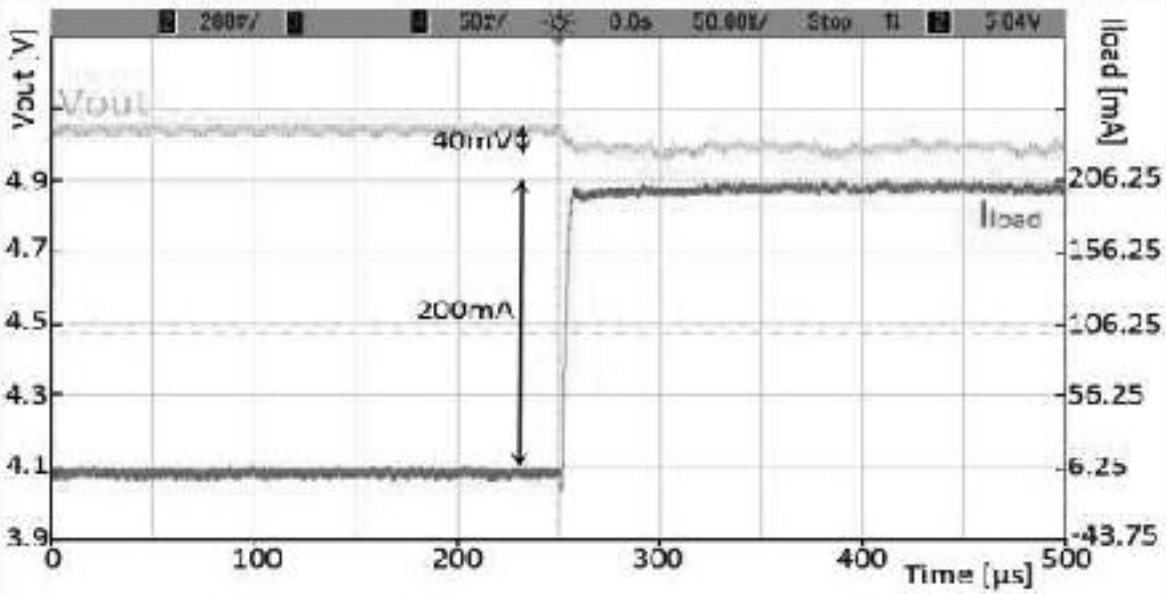
WP5: V2 line and load regulation



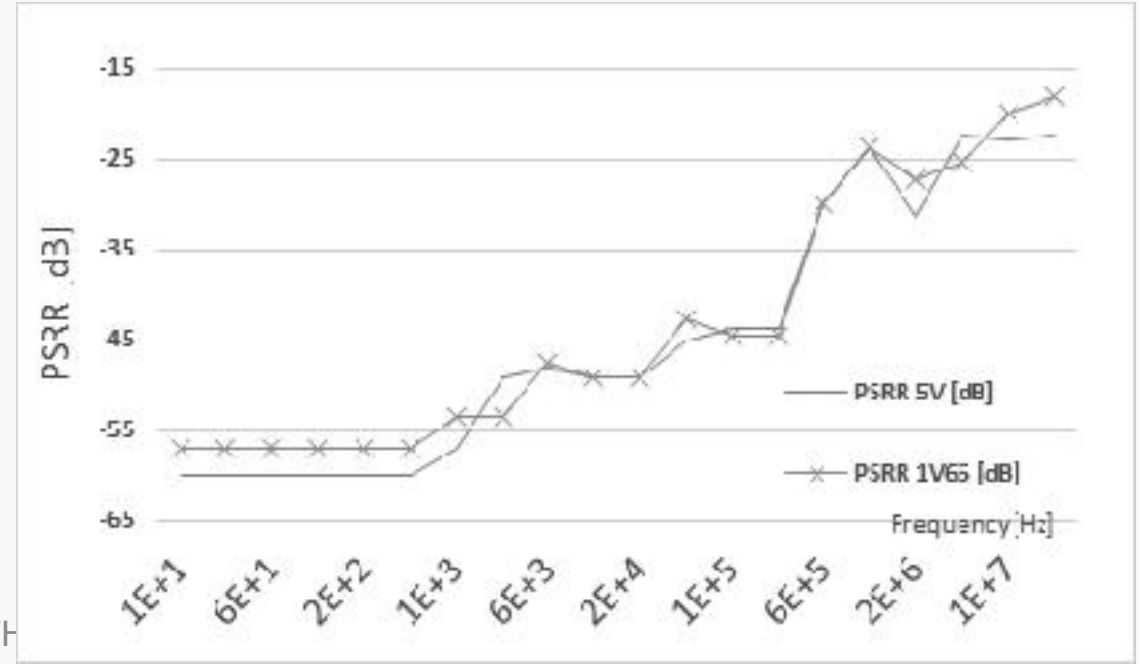
Good line and load regulation performance



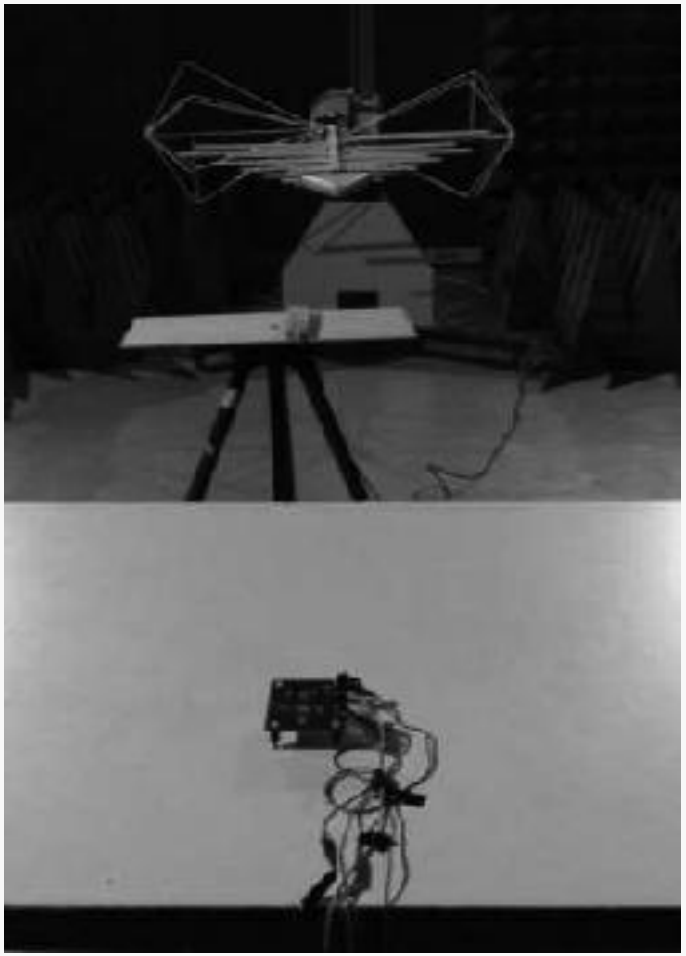
WP5: V2 transient response and PSRR

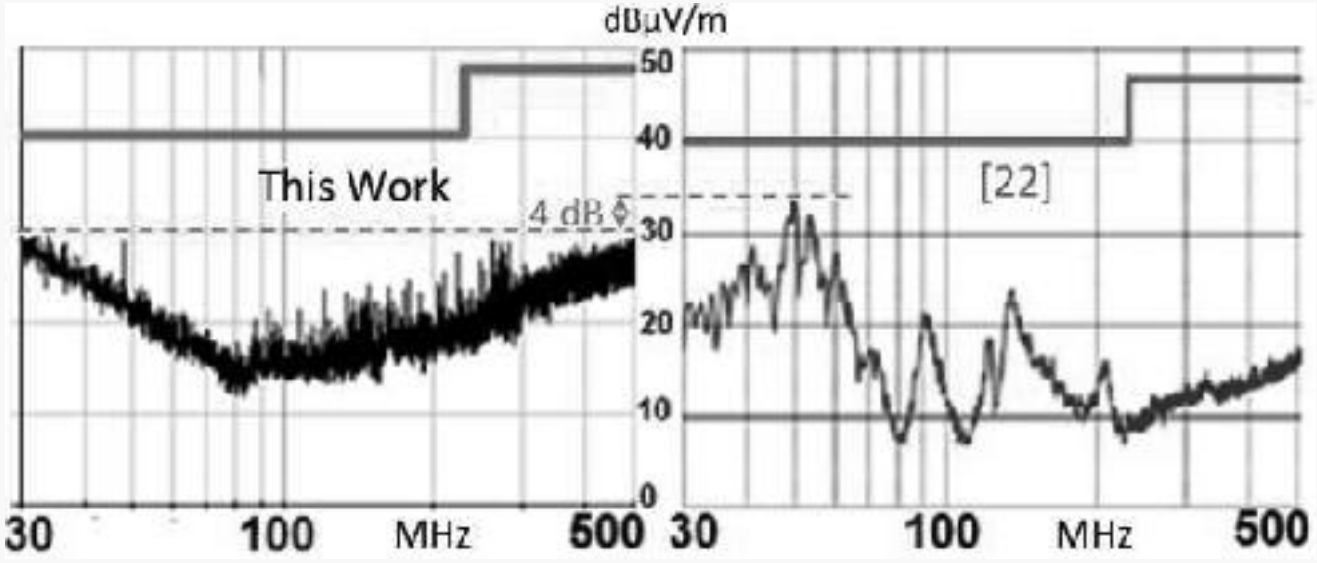


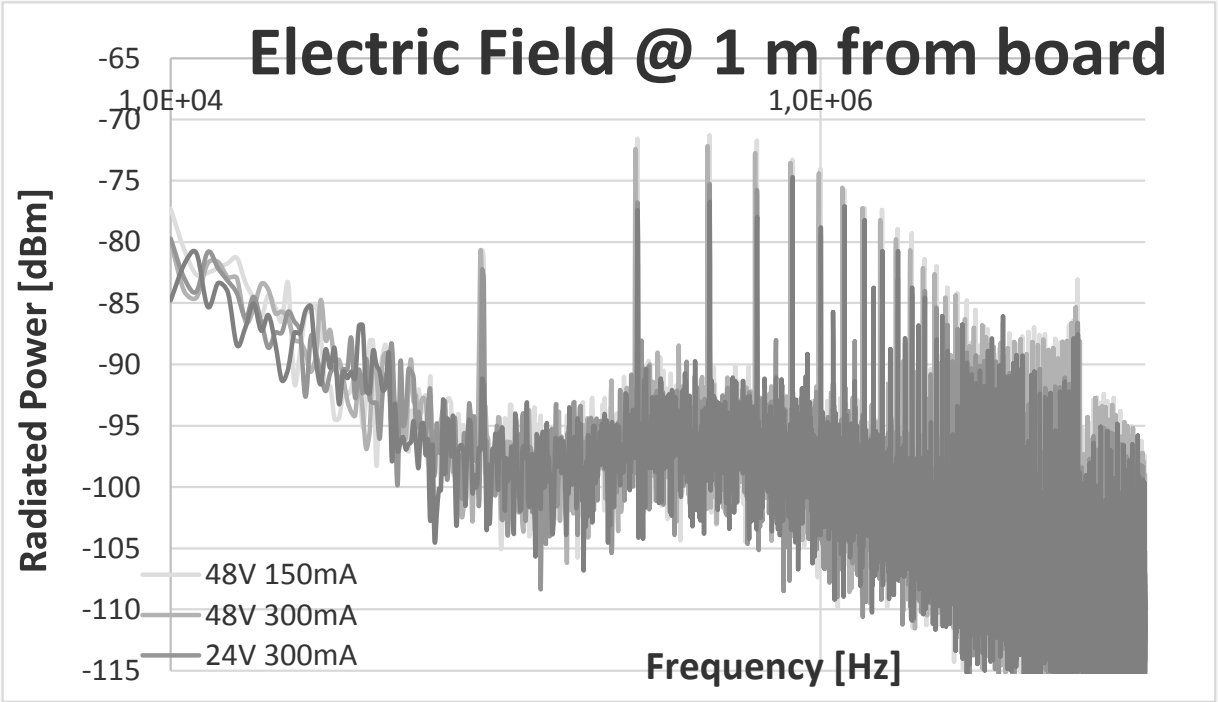
Good transient and PSRR performance



WP5: V2 radiated EMI

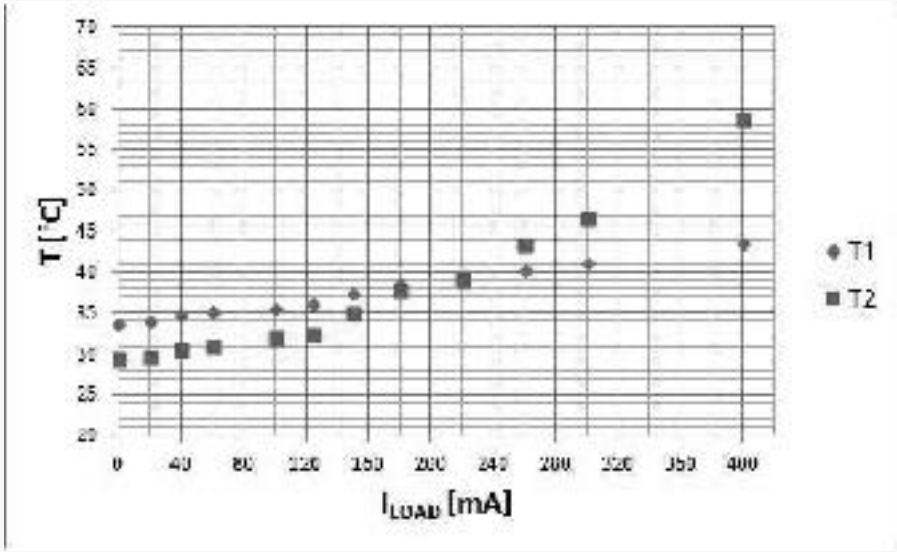






Low radiated EMI

WP5: Temperature tests and state-of-art review

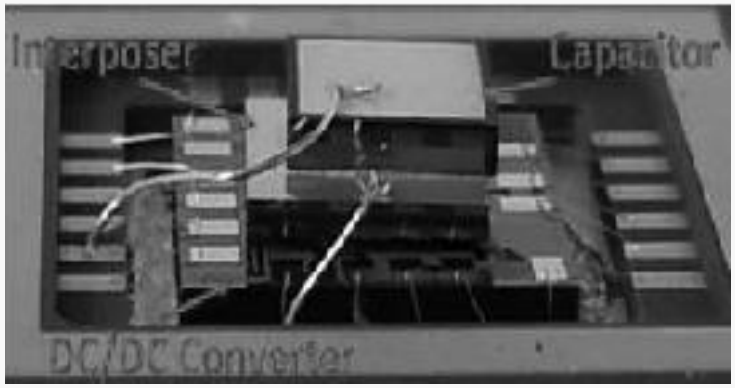


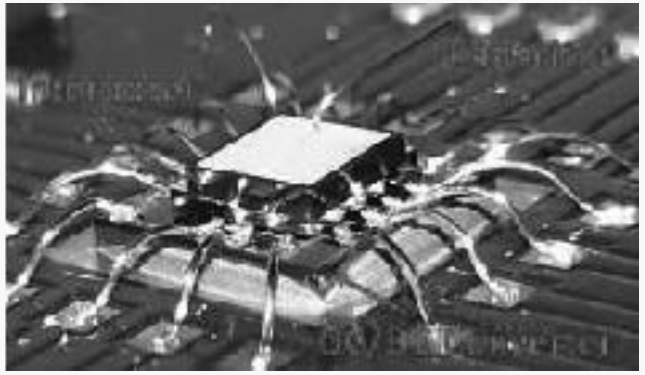
Low over-temperature (can work also without cooling system)

Integrated LDO, I/O insulation and wide input range vs. state-of-art

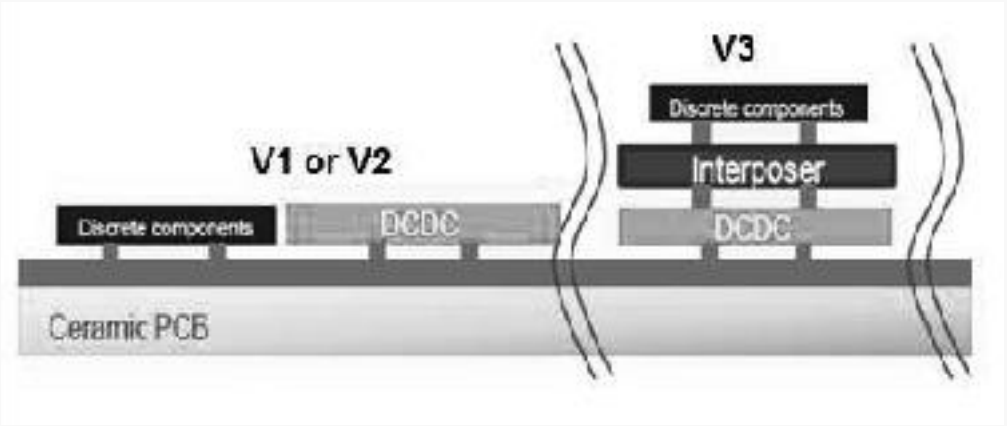
	This Work	PT4660	LT3245	LM5170
Type	SC+linear	Inductive	SC	Inductive
In-Out insulation	Yes	Yes	No	No
Input range [V]	57*	39	35	79
PSRR [dB]	-60	Off-chip LDO needed		
Output voltage [V]	1.65 / 5	3.3 / 5	5	12 / 48
Max load current [A]	0.4	30	0.25	5
Efficiency peak [%]	63	86	81	N/A
Stand-by current [μA]	5	5000	4	10

WP5: V3 with capacitors stacked on top





Unaltered performance of V3 vs. V2 but much lower area



T5.3: Advanced control techniques for 48V DCDC using IPDs [Leader: UNIPI]

Start: M7

End: M40

Objectives:

O5.3: Develop advanced control techniques for 48V DCDC using IPDs.

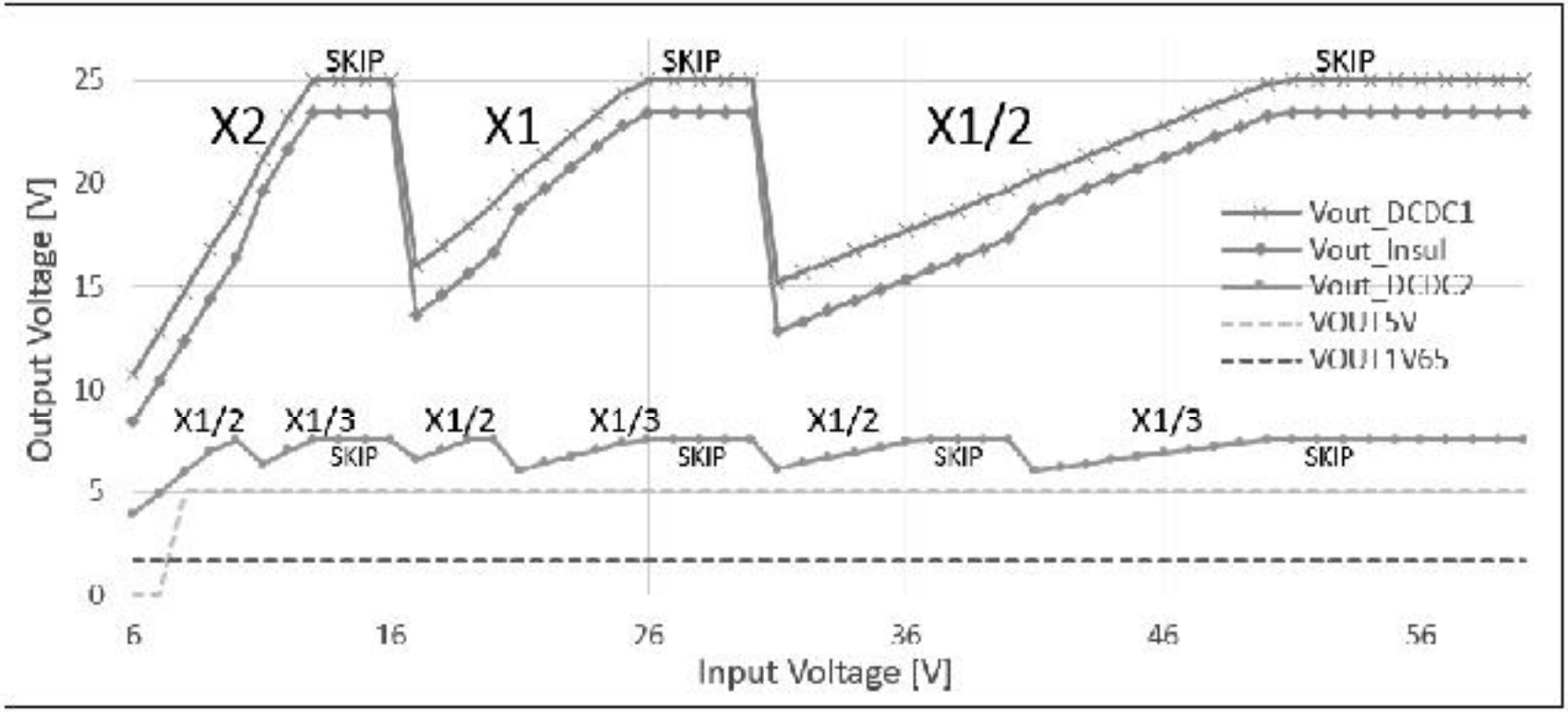
Status

- Design of advanced control techniques (Topology reconfiguration, Skip control, switching frequency spreading, anti-EMI filter, soft-start, gate driving slope control) implemented in the 3 chip versions of T5.2, and fully characterized to reduce EMI (thus improving EMC), while keeping good performance in terms of line regulation, load regulation, ripple, PSRR, thermal behaviour with a signal quality comparable to linear regulators but with a much better power efficiency when regulating high input voltages (up to 60V) to load power loads (e.g. 5V and 1.65V such as sensors, memories and processors in ECU)

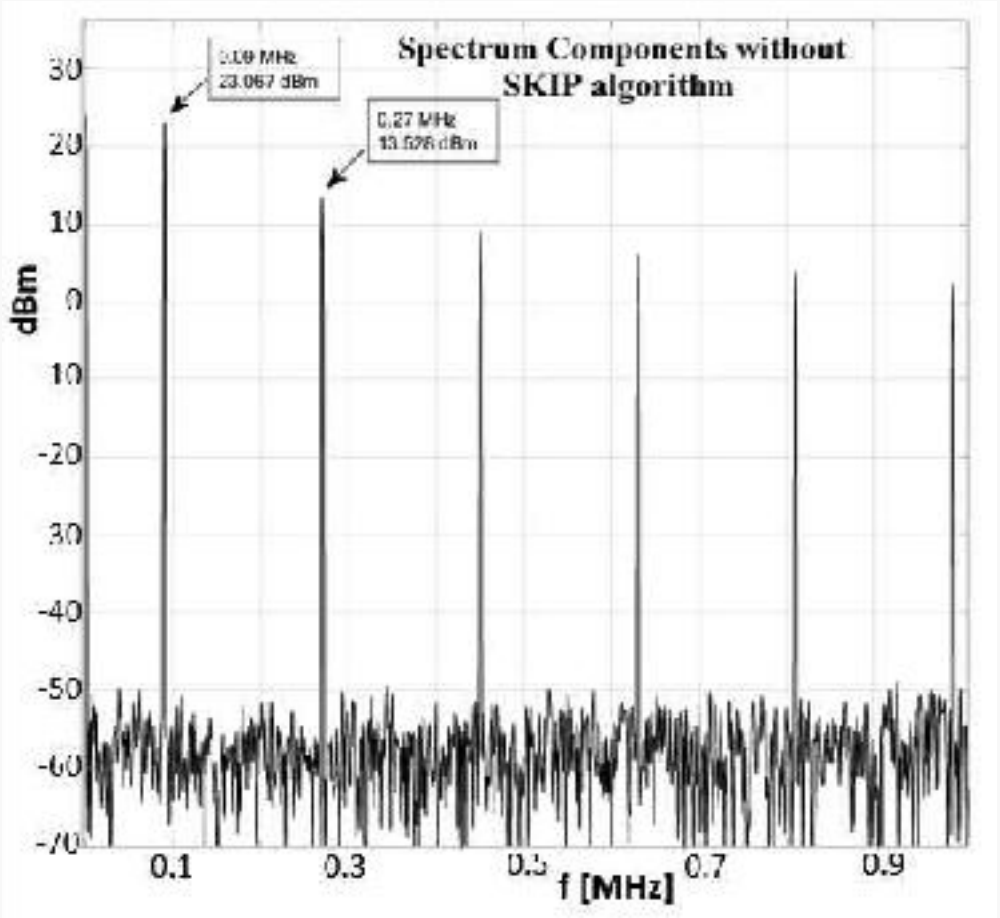
WP5: Topology reconfiguration

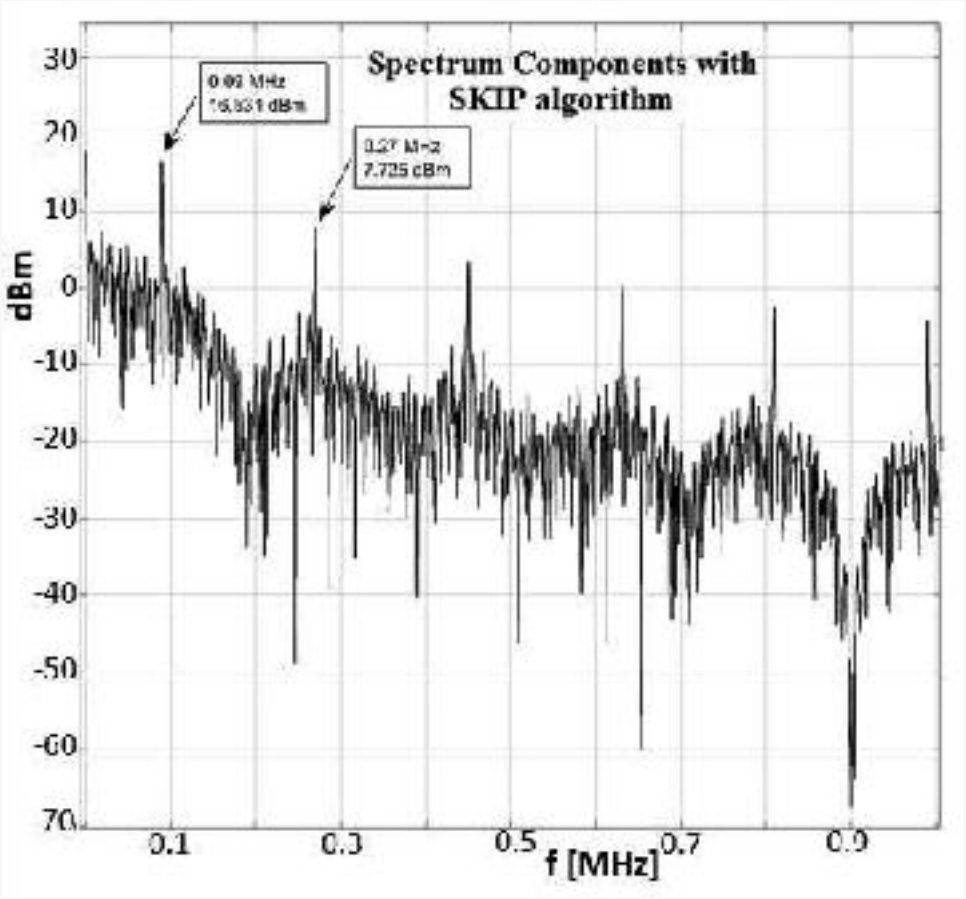
Stage	Input Voltage [V]	VCR	Output Voltage [V]
DCDCA	6 < Vin < 15	2	12 < Vout < 30
	15 < Vin < 29	1	15 < Vout < 29
	29 < Vin < 60	1/2	14.5 < Vout < 30
ISOL	12 < Vin < 30	1	12 < Vout < 30
DCDCB	12 < Vin < 18	1/2	6 < Vout < 9
	18 < Vin < 30	1/3	6 < Vout < 10
LIN_1	V_X > 6	-	5
LIN_2	V_X > 3	-	1.65

Effects of the control techniques (topology reconfiguration and SKIP-mode on the voltage regulation in the multi-stage DC/DC architecture)

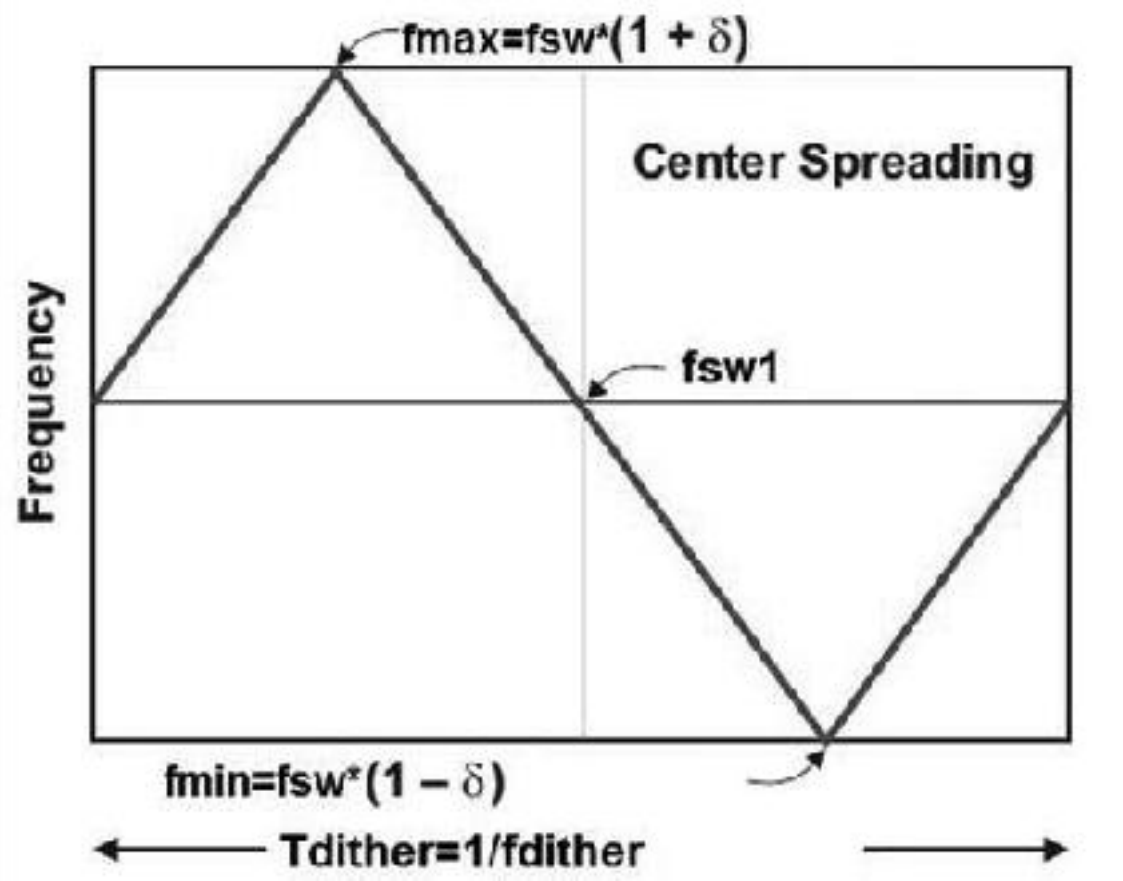


More than 6 dB reduction of the EM Interference power emission thanks to SKIP-mode. Fixed frequency, like a PWM with duty-cycle hopping between 0.5 and 0

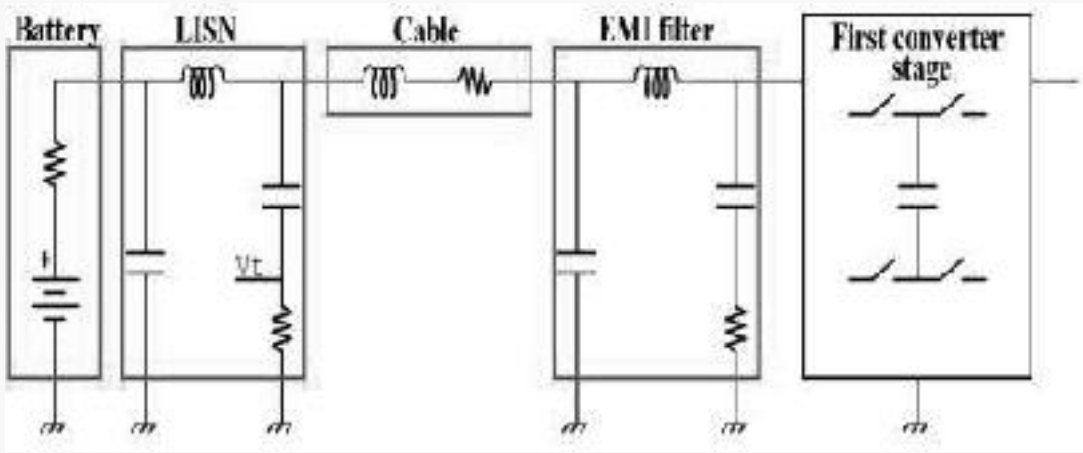


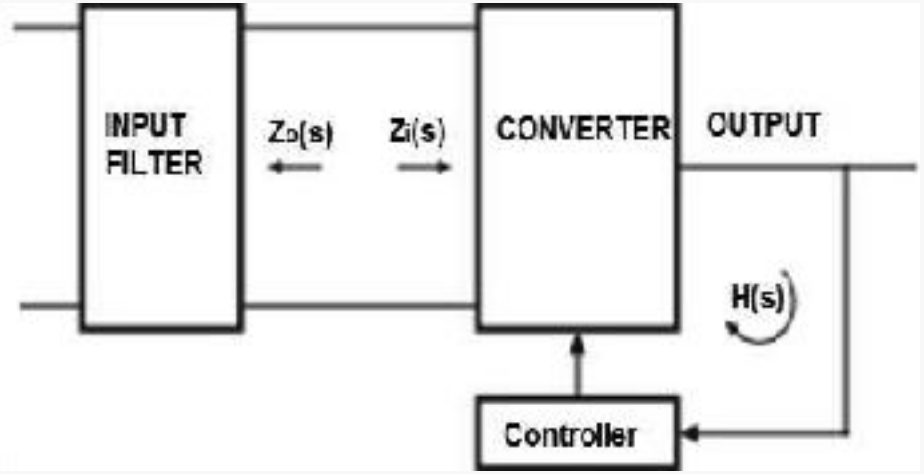


WP5: Switching frequency spreading

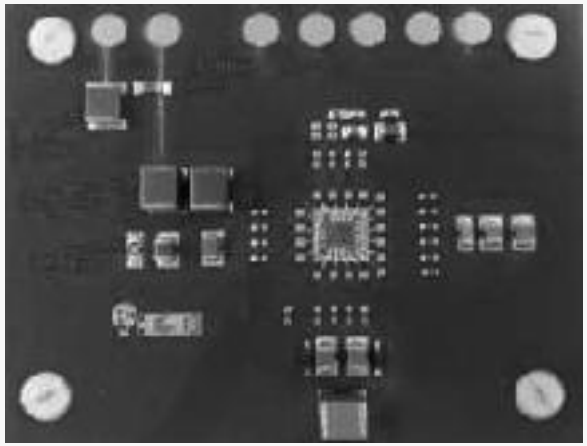


*Extra spectral attenuation (dB)=10*log[(f_{SW}*δ)/(f_{DITHER}/n)]*





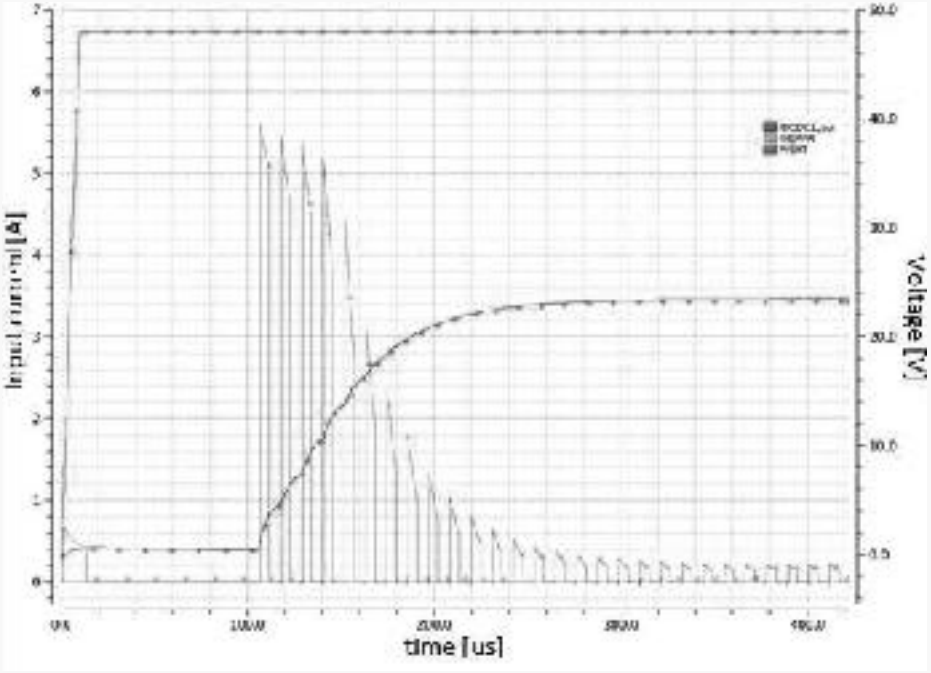
The design of anti-EMI filter aware of input converter impedance allows reducing x 3 the size of the filter components and avoids instability

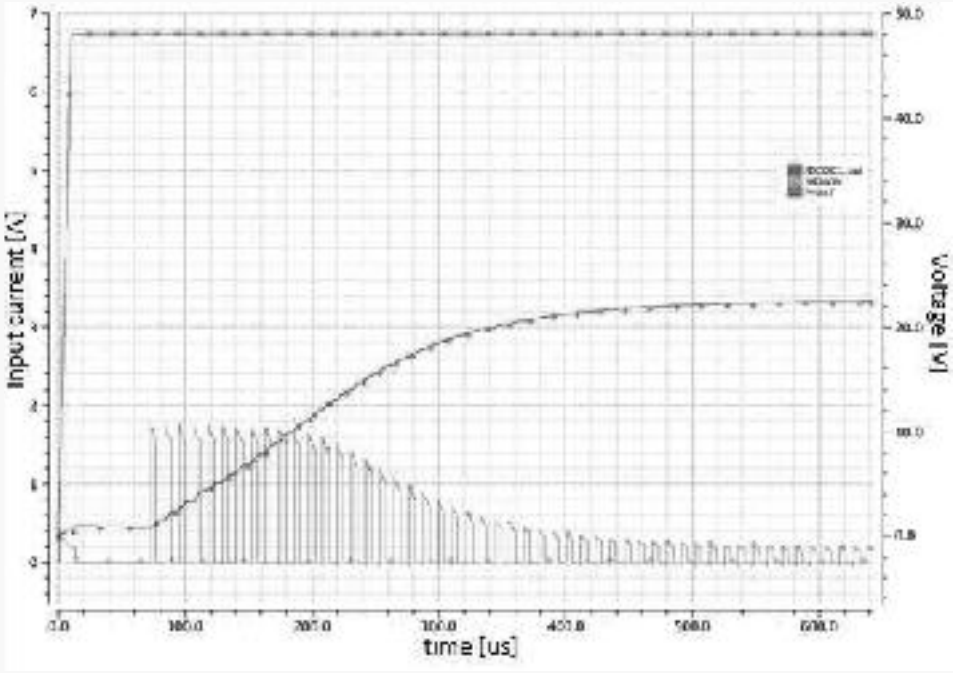


	Set-up		EMI measurement results	
	$V_{battery}$,[V]	I_{load}, [mA]	Freq.peak., [kHz]	Amplitude, [dBV]
This work	8	0-300	180	-84, -74.8, -65.4
	12	0-300	180	-87.2, -77.4, -69.8
	24	0-300	180	-77.8, -77.2, -75.4
	48	0-300	160	-74.4, -76.4, -71.4
	60	0-300	100	-71.4, -63, -57.8
[TI]	30	1600	10	-47.5

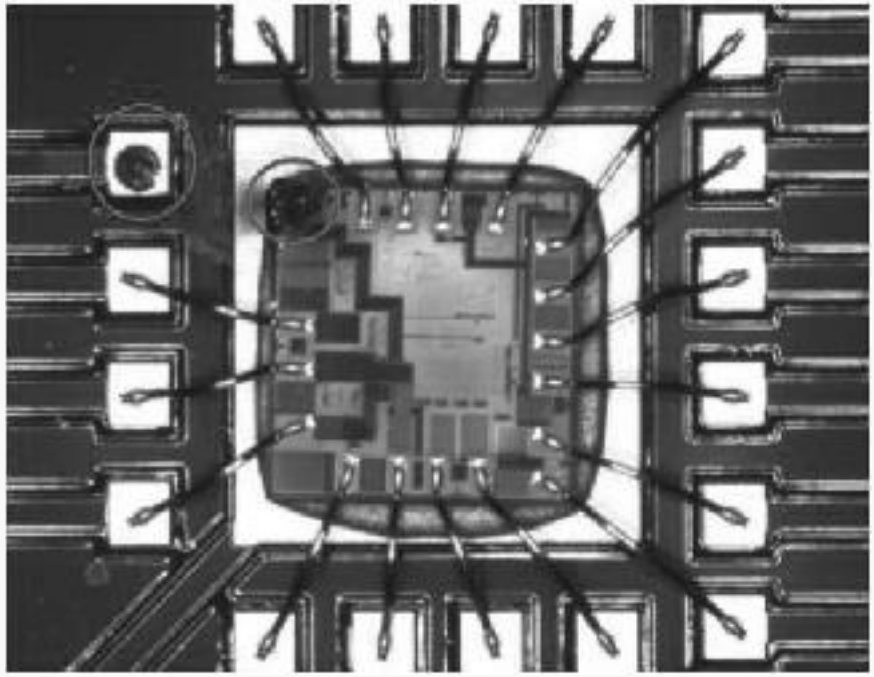
Input current without/with soft-start modality (the current peaks, represented from green signal, are reduced by 3 times).

HV-MOS are realized as multiple parallel devices, activated according to a proper sequence when starting to avoid high in-rush currents





Without soft-start chip can be damaged by high current peaks at device start



	Conducted EMI reduction	Radiated EMI reduction	Could be integrated	Low design effort	Low cost
EMI filter	+ + +	-	- -	- -	**- -**
SKIP control	+ +	+ +	+ + +	+	**+ +**
Soft-Start technique	**+**	**+**	**+ + +**	**-**	**+**

WP5: Main Publications on Journals

- **Saponara, S.,** Tisserand, P., Chassard, P., My-Ton Dieu, “Design and Measurement of Integrated Converters for Belt-driven Starter-generator in 48 V Micro/mild Hybrid Vehicles”, **IEEE Transactions on Industry Applications**, July issue, pp. 1-13, 2017, DOI: 10.1109/TIA.2017.2687406
- **Saponara, S.,** Ciarpi, G., “Design and experimental measurement of EMI reduction techniques for integrated switching DC/DC converters”, **IEEE Canadian Journal of Electrical and Computer Engineering**, vol.40, n.2, 2017, DOI: 10.1109/CJECE.2017.2703107
- **Saponara, S.,** Fanucci, L., Biagi, E., Serventi, R., “Hard macrocells for DC/DC converter in automotive embedded mechatronic systems”, **EURASIP Journal on Embedded Systems**, vol. 2017, n. 1, DOI: 10.1186/s13639-016-0044-8, pp. 1-13
- **Saponara, S.,** Ciarpi, G., “IC Design and Measurement of an Inductorless 48 V DC/DC Converter in Low-Cost CMOS Technology Facing Harsh Environments”, **IEEE Transactions on Circuits and Systems I**, 2017, pp. 1 - 14, DOI: 10.1109/TCSI.2017.2713702
- Saponara, S., Ciarpi, G., “IC Design and Measurement of an Inductorless 48 V DC/DC Converter in Low-Cost CMOS Technology Facing Harsh Environments”, **IEEE Transactions on Instrumentation and Measurements**, 2017, submitted

WP5: Main Publications on Conferences

•Sisto, A., **Saponara, S.**, Ciarpi, G., Iacopetti, F., Fanucci, L., “Testing of DC/DC Converters for 48 V Electric Vehicles”, Chapter 20 in Lecture Notes in Electrical Engineering, vol. 429, 2017, Springer, ISBN 978-3-319-55070-1, doi: 10.1007/978-3-319-55071-8_20

• **Saponara, S.,** Ciarpi, G., “Electrical and Electromagnetic Measurements of an Inductorless DC/DC Converter”, IEEE Int. Instrumentation and Measurement Technology Conference (I2MTC) 2017, Torino, I, 22-25 May 2017, pp. 27-32, ISBN 978-1-5090-3596-0

• **Saponara, S.,** Ciarpi, G., “Universal and inductorless DC/DC converter for multi-output power supplies in sensor and actuator networks”, Proceedings of SPIE Microtechnologies, vol. 10246, pp. 1-6, Barcelona, 8-10 May 2017, doi: 10.1117/12.2265188, pp. 1024612-1 1024612-6

• **Saponara, S.,** Ciarpi, G., Mattaliano, C., Fanucci, L., Groza, V., “Improving Electromagnetic Compatibility of Integrated Switching Converters for Hybrid/electric Vehicles”, IEEE EPEC 2016, pp. 1-6, doi: 10.1109/EPEC.2016.7771733

•**Saponara, S.,** Fanucci, L., Mattaliano, C., Ciarpi, G., Sisto, A., Neri, B., “48 V DC/DC switched-cap converter for hybrid/electric vehicles”, GE 2016

•**Saponara, S.,** Moras, R., Roncella, R., Saletti, R.,Benedetti, D., “Performance measurements of energy storage systems and control strategies in real-world e-bikes”, IEEE Sensors Applications Symposium (SAS), pp. 379-384, 2016, doi: 10.1109/SAS.2016.7479876

WP5: Main Publications on Conferences

• Wachmann, E., **Saponara, S.,** Zambelli, C., Tisserand, P., Charbonnier, J., Erlbacher, T., Gruenler, S., Hartler, C., Siegert, J., Chassard, P., Ton, D.M., Ferrari, L., Fanucci, L., "ATHENIS_3D: Automotive tested high-voltage and embedded non-volatile integrated SoC platform with 3D technology", IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 894-899, 2016,

•**Saponara S.,** Tisserand, P., Chassard, P., My-Ton, D., "DC/DC converter integrated architecture for 48V supplies in micro/mild hybrid vehicle electrical engine control module", pp. 1-5, IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC), 2016, doi: 1109/EEEIC.2016.755585

Dissemination of the activity results also at GE2015, I2SC2016, WISP2015, WF-IoT2015, SPIE 2016, SPIE2015