WP4: 3D TSV & WLP MODULE DEVELOPMENT

Leader: **CEA-Léti (CEA) - Jean Charbonnier (jean.charbonnier@cea.fr)**

Start: M4 - 20.03.2014

End: 03.2017

WP4 planned effort and Deliverables

Updated DoW

Work package		AMS	VEEM	Crocus	FHG	TUW	UNIFE	AT	MASER	BESI	CEA	UNIPI	Total
WP4	Planned person.months per participant	20,0			28,0	20,0			1,0	18,0	56,6		143,6

Deliverables

D4.1: M6 ✓ Report Requirements and specifications for simulation of process technology and electrical, thermal, and mechanical behaviour of integration structures [AMS]

D4.2: M8 ✓ Report Simulation concepts, materials, stress measurements [FhG]

D4.3: M17 ✓ Report TSV, Power Cu and solder process modules implemented [CEA]

D4.4: M29 ✓ Report Process module updates for final 3D/TSV/WLP technology concept [CEA]

D4.5: M32 ✓ Report TSV and WLP process simulation methodology [FhG]

D4.6: M36 ✓ Report on Wafer Level Molding [CEA]

Milestone

MS3: M17 Development of process modules for platform integration completed

WP4: Partner Contributions

Partner 1: ams

Project leader for 3D platform, global base technology development

Partner 4: FHG

Simulation (TCAD), Test vehicle definition

Partner 5: TU Vienna

EM Simulation (specific software modules)

Partner 8: Maser Engineering

Physical failure analysis and reliability testing expertise

Partner 9: Besi

Chip to wafer stacking process development : SB2 and WLSST, global assembly.

Partner 10: CEA

Base technology development for Power Cu TSV and Thick RDL and Chip to wafer interconnection.

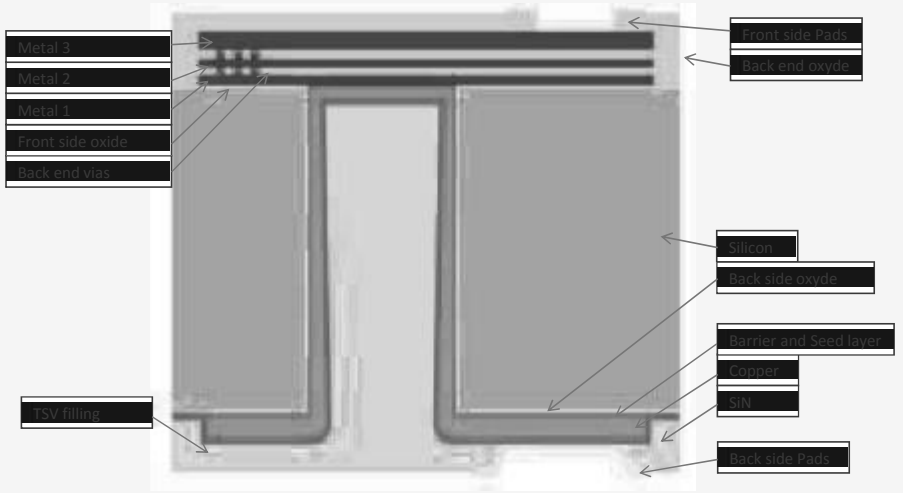
Test vehicle process for all copper technology

WP4: Task 4.1 Overview

T4.1: Development of TSV last process module for automotive requirements [Leader: CEA]

Start: M4, 20.03.2014

End: M27, 20.02.2016



Through Silicon Via (TSV) last Integration scheme

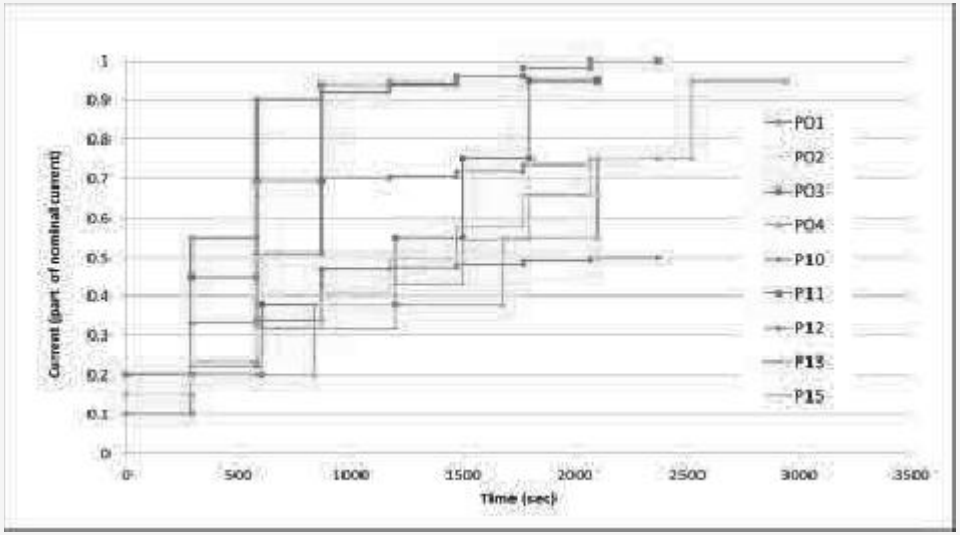
Objectives:

- Development of Cu TSV technology of Aspect ratio 2,5:1 (diameter 80µm, height 200µm) for high currents and temperature (200C).
- Increase the TSV aspect ratio from 2.5:1 to 5:1 with respect to current and thermal specifications.
- Optimization of TSV reliability to thermal cycling and mechanical stress using design, dielectric and organic materials benchmark according to simulation (T4.4).

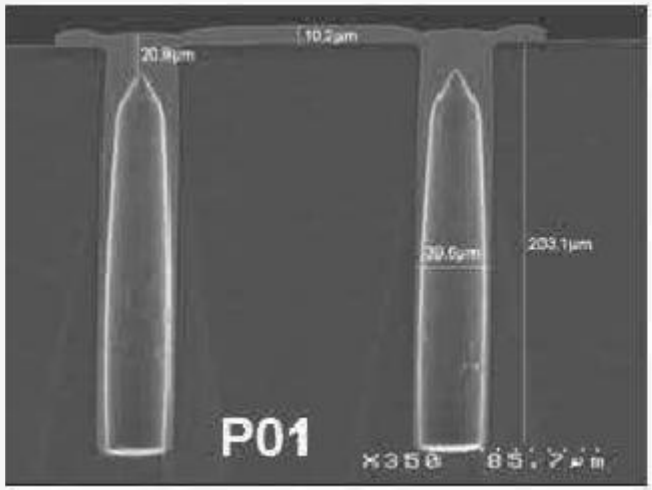
WP4: Task 4.1 – Zoom on Cu TSV study

TSV 40x200µm DOE

Cu ECD recipe process profiles



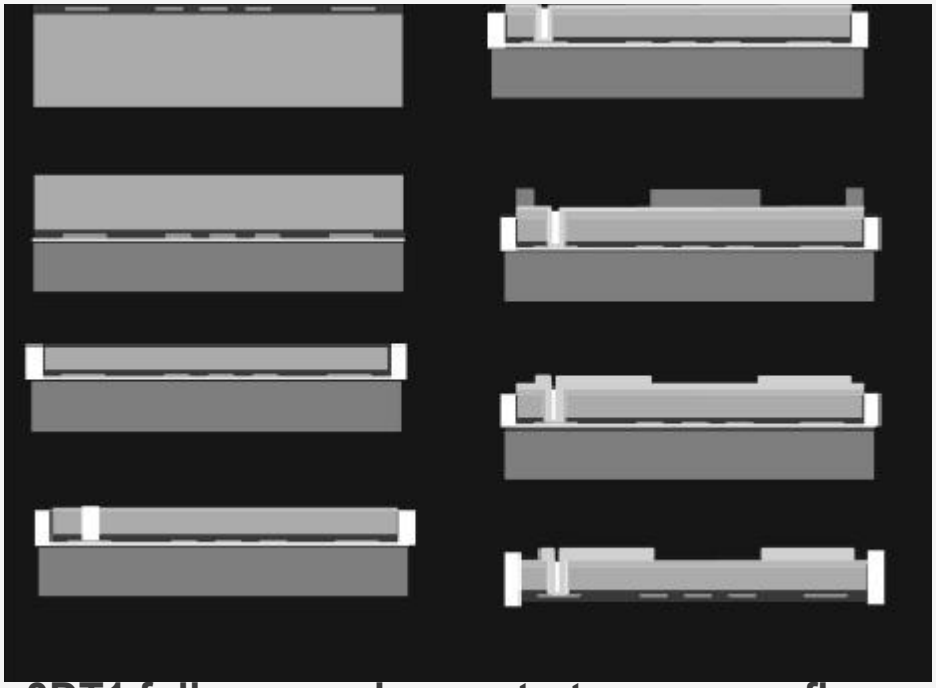
Closing phenomenon



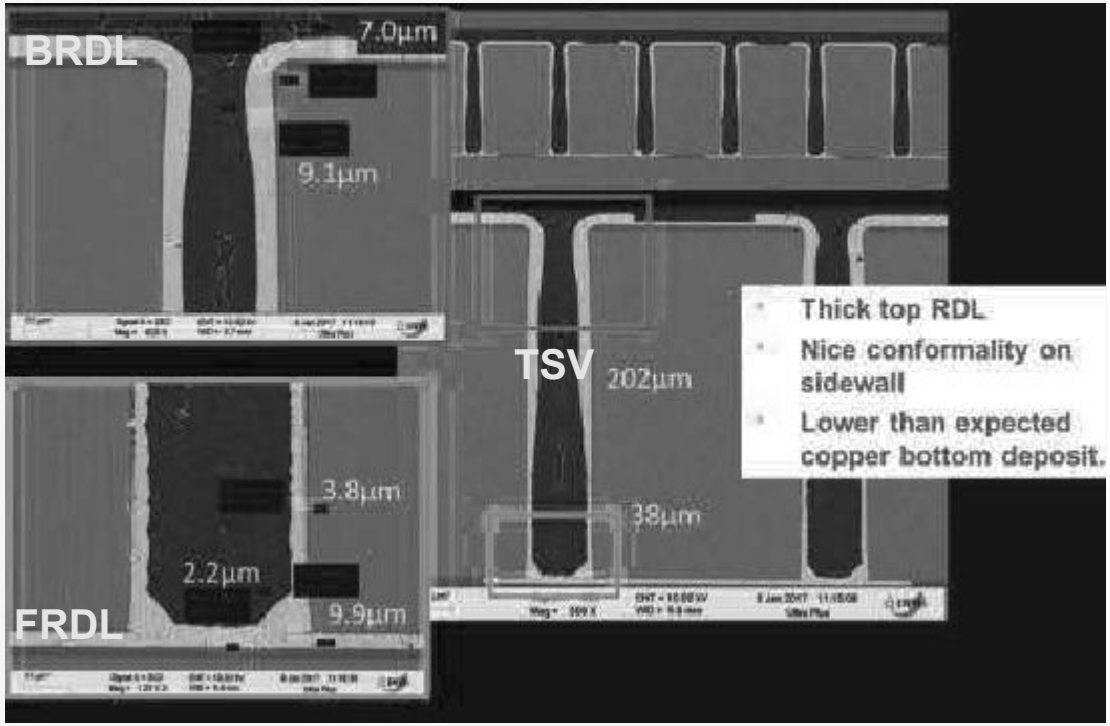
Best Known Method

Top sidewall broadening

TSV 40x200µm integration

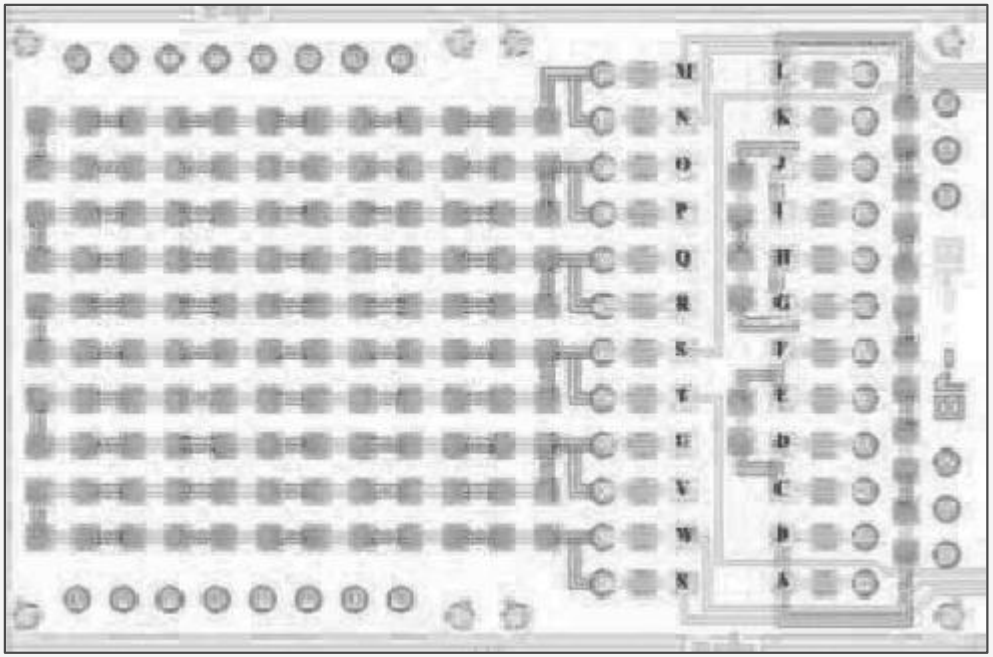


3DT1 full copper demonstrator process flow



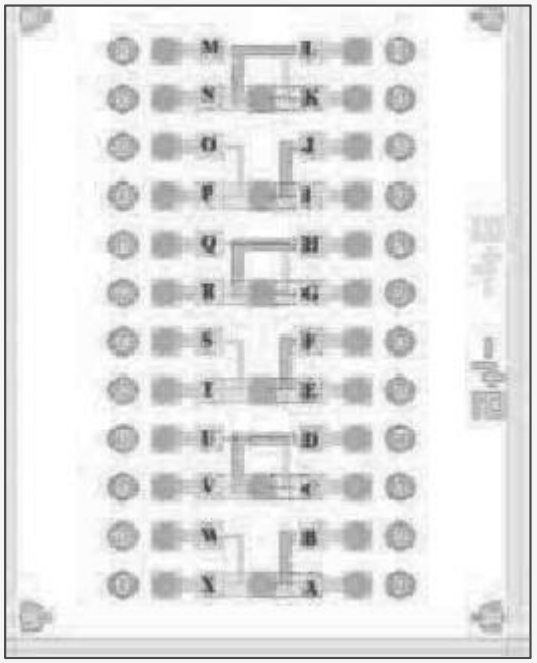
Cu ECD TSV Process integrated in electrical demonstrator

Tests patterns



TSV Chains (MT18)

TSV diameter



Ø 42µm

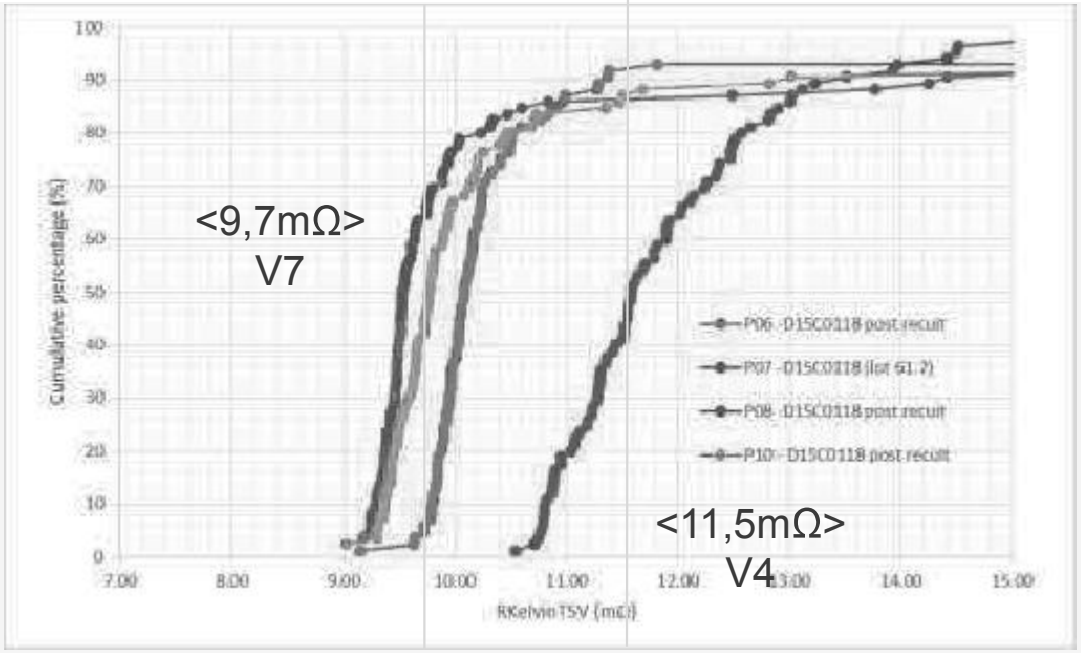
Ø 40µm

Ø 38µm

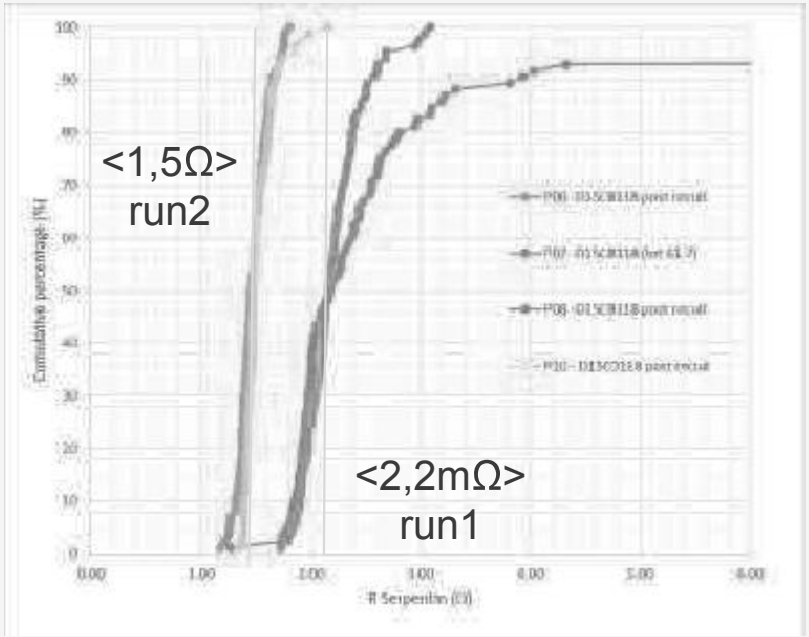
TSV Kelvin (MT46)

WP4: Task 4.1 –Cu TSV study - Power Process

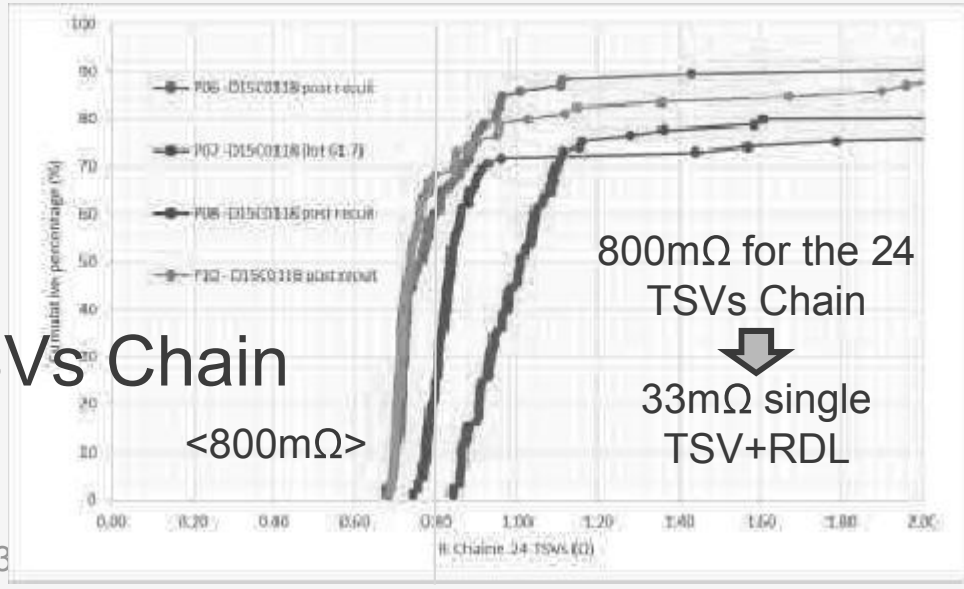
TSV Kelvin



BRDL Serpentine



24 TSVs Chain



T4.2 Development of thick copper metallization process for high current density [Leader: CEA]

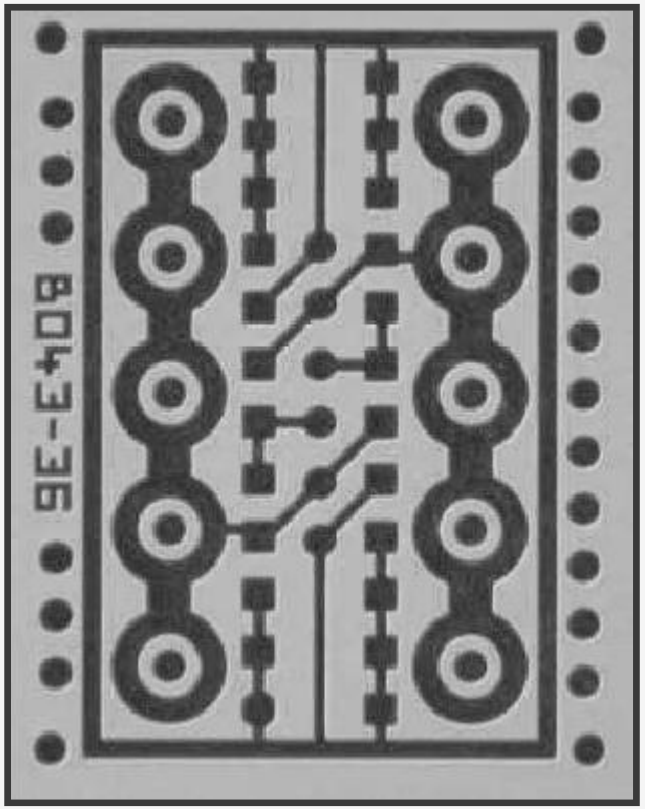
Start: M4, 20.03.2014

End: M27, 20.02.2016

Objectives:

-Process development of a thick (≥10µm) Cu backside redistribution layer (BRDL) for high currents and temperature (200C) – Line/Space= 20/20µm.
-Deliver a Test vehicle for BRDL evaluation (Imax, leakage current, and breakdown voltage evaluation).
-Optimization of BRDL reliability to thermal cycling and mechanical stress using design, dielectric and organic materials benchmark according to simulation (T4.4).

➔ BRDL Passivation focus for copper corrosion protection



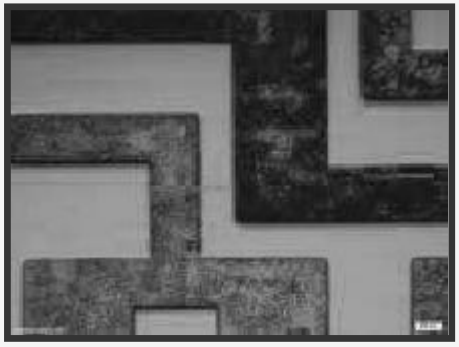
RDL Cu 9µm before passivation

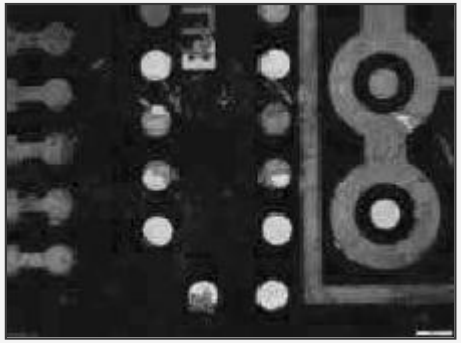
(3DT1 test pattern)

MASER TEST CAMPAGNE – 200 ° C FOR 590H

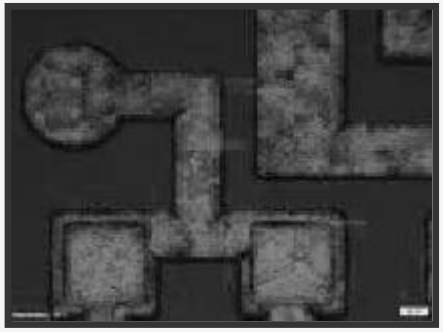
- HTS at 200 °C for 590h at Maser, non controlled atmosphere
- Traget copper thickness 3µm - Profilo P16 - Mean : 2.6 Min: 2.4 Max: 2.8µm
- Copper annealing Etuve 101- 350°C 60min (Profil 8)
- Wet etch of barrier/seed

Reference: RDL Cu wo passivation P02

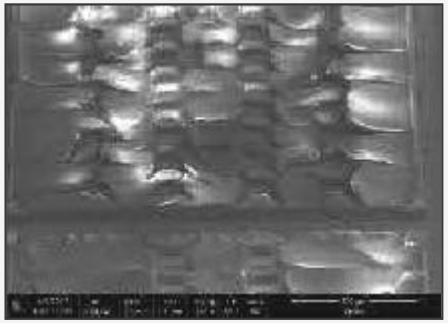




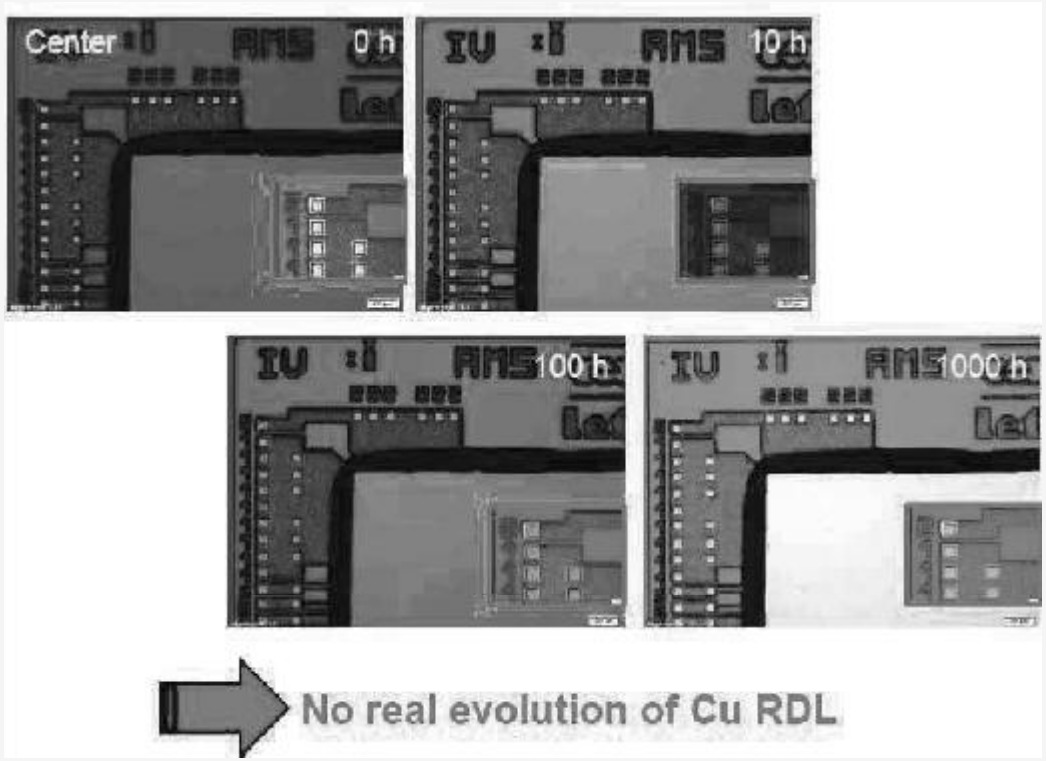
Option 1: passivation SiNconf-300° C P03



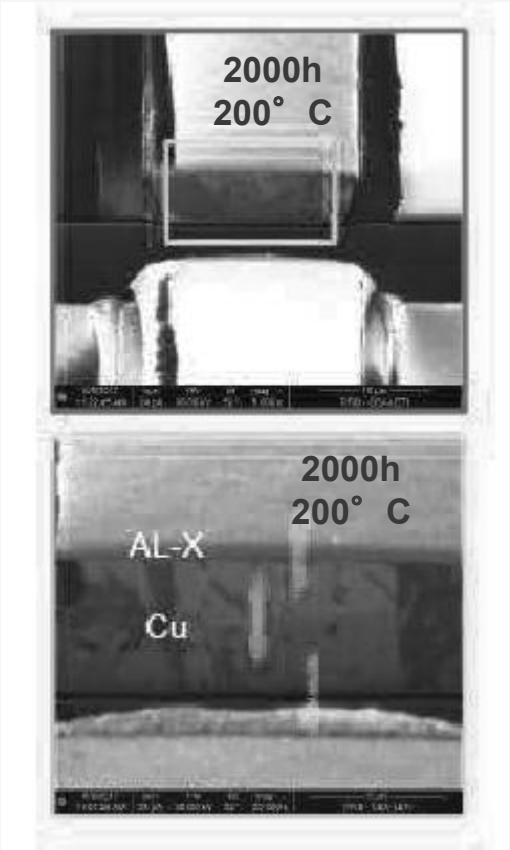
Option 2: (no deox) passivation SiNR 3170 50µm P06 (cure SiNR 2h at 120° C + 2h at 180° C)



OPTIMIZED PASSIVATION: SIN + ORGANIC

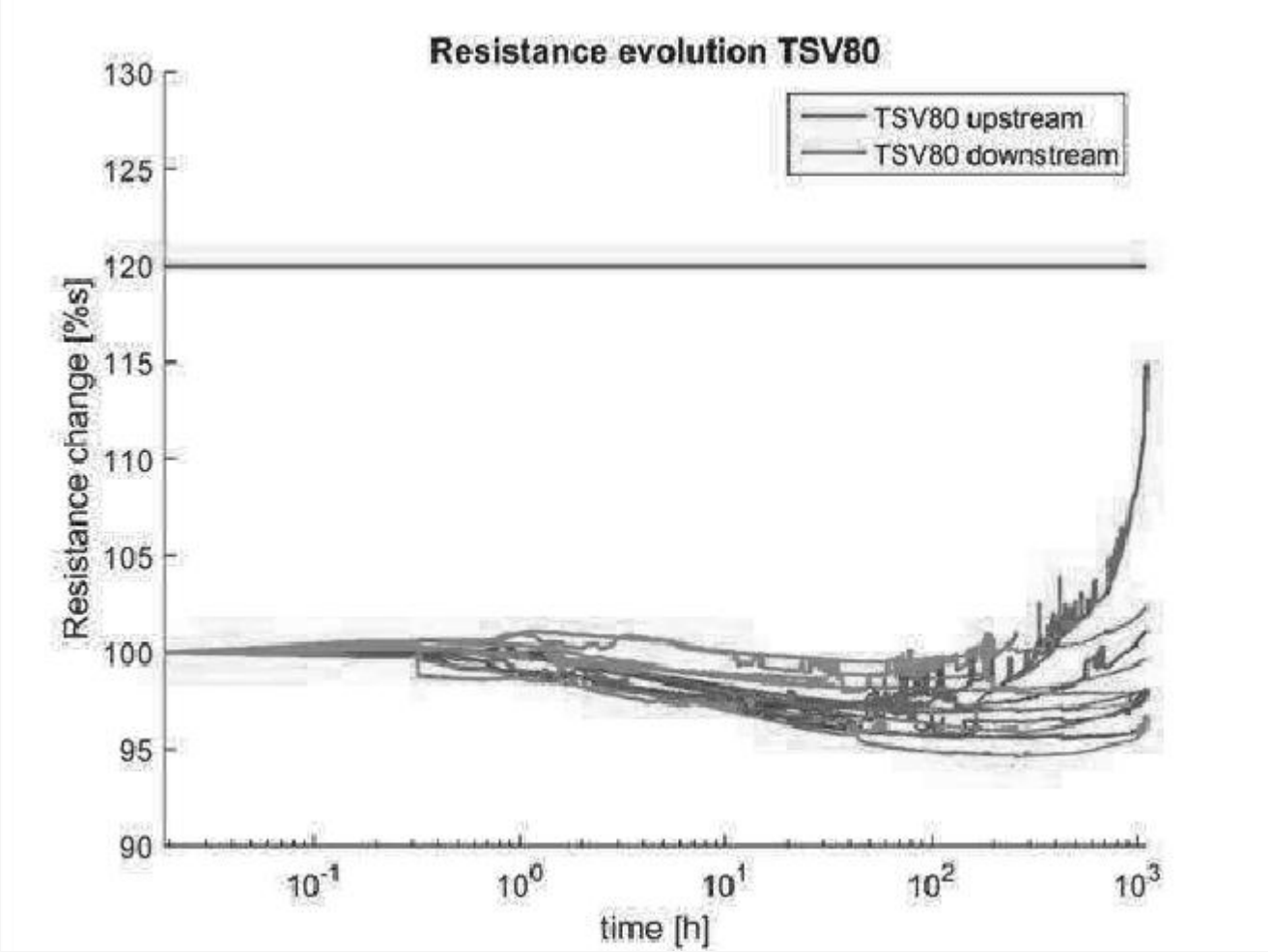


for more than 2000h
at 200° C.



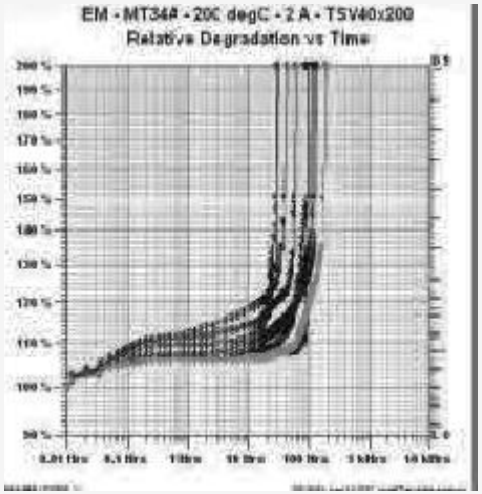
→ 100nm SiN + organic have been chosen as a standard integration for all the reliability lots and demonstrator.

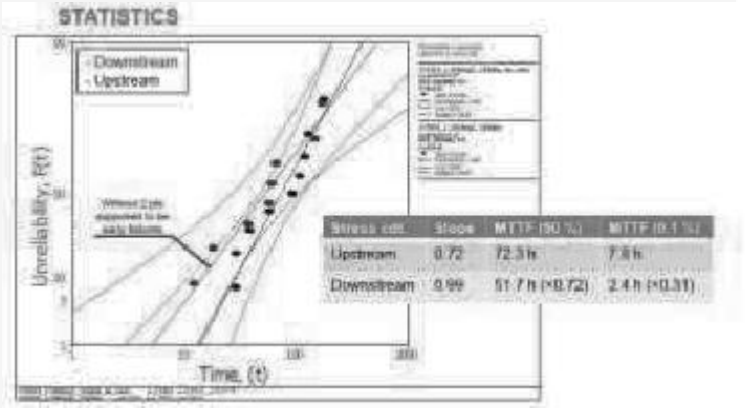
RDL+TSV HTS & TESTS

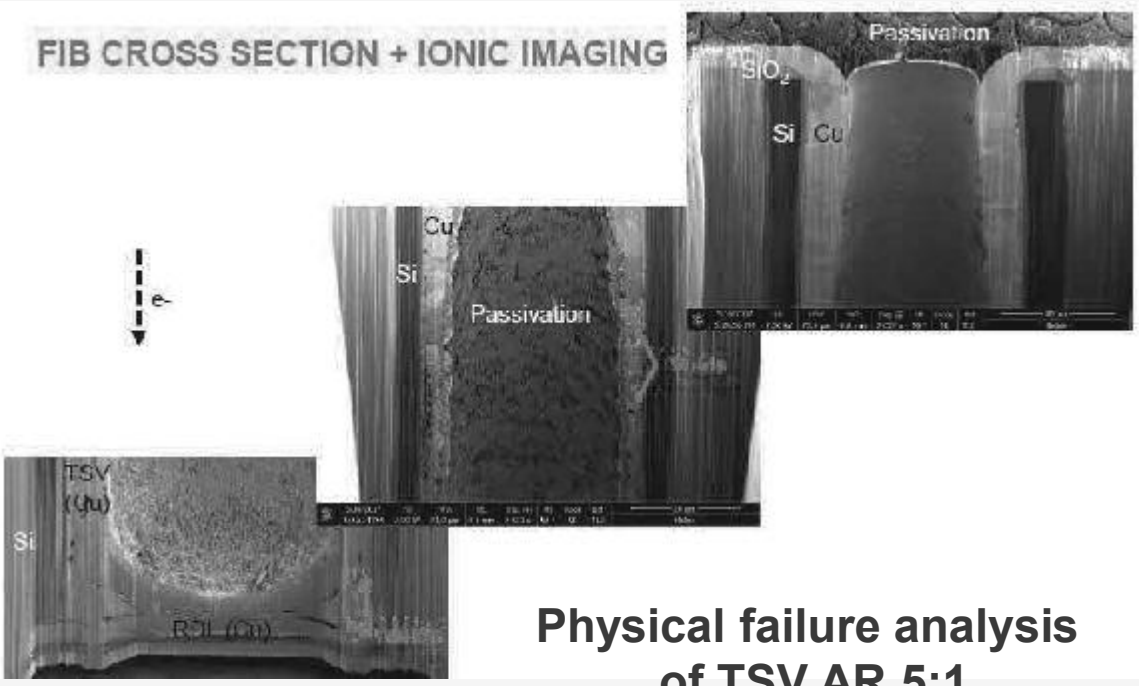


➔ Validation of the RDL + TSV modules for more than 2000h at 200° C.

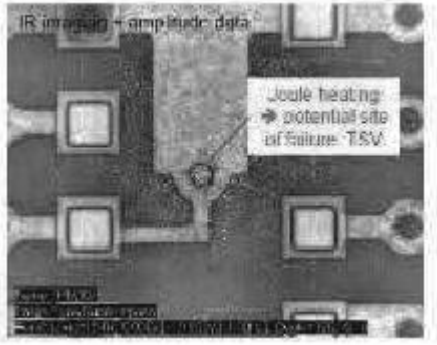
RDL+TSV HTS & EM TESTS







Physical failure analysis of TSV AR 5:1



RESULTS & CONCLUSION

Results & Observations

AR 2.5:1 (TSV 80x200µm):

- A recipe has been developed and optimized with polyvalent chemistry.
- From an industrial point of view the chemistry used is low cost and can be used for copper damascene, copper pillars process also.

AR 5:1 (TSV 40x200µm):

- A bottom up process has been qualified on TSV 40x200 with success.
- The process has been tune especially for power and high current density.

RDL & Passivation

- 10µm Thick CU RDL process has been stabilized (Flow and annealing optimization.
- A full Doe on passivation permit to integrate an efficient solution.

Conclusion

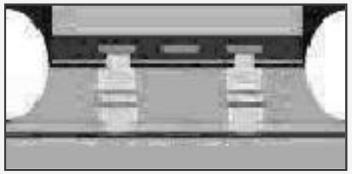
- High temperature test have been validated and project specifications overpassed (200°C-100°C) for thick RDL and TSV modules
- EM void location and failure mechanism have been identified and quantified.

WP4: Task 4.3 Overview

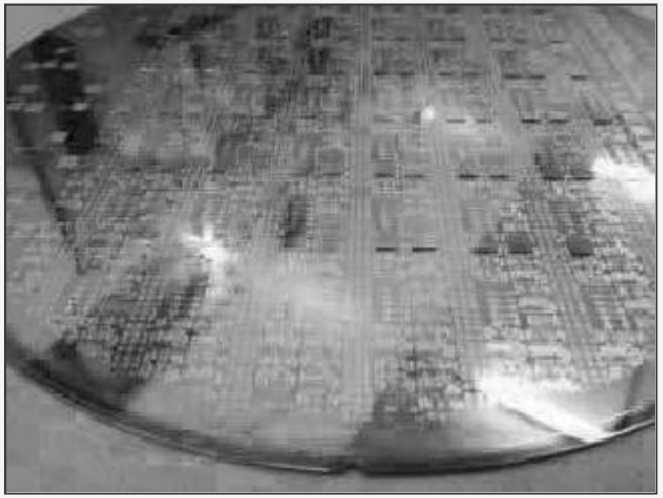
T4.3 Development of WLP process modules for automotive requirements [Leader: AMS]

Start: M4, 20.03.2014

End: M27, 20.02.2016



Schematic cross section of WLP device (top and bottom die, copper bumps/pillars interconnection)



Objectives:

- Demonstrator structure proposal
- Choice for each chip interconnection
- Test structures definition, test vehicle design
- Test vehicle process and tests: DC and Reliability
- Simulation and experimental results: optimization of stacking process and integration to meet the thermal specification of -55C to 200C especially concerning UBM and Solder materials
- Decrease of ball or bump size from 80µm to 15-20µm while keeping the same robustness to thermal stress
- Bumping process on prototypes for other tasks and WPs and final demonstrator stacking (Leti, BESI, AMS)

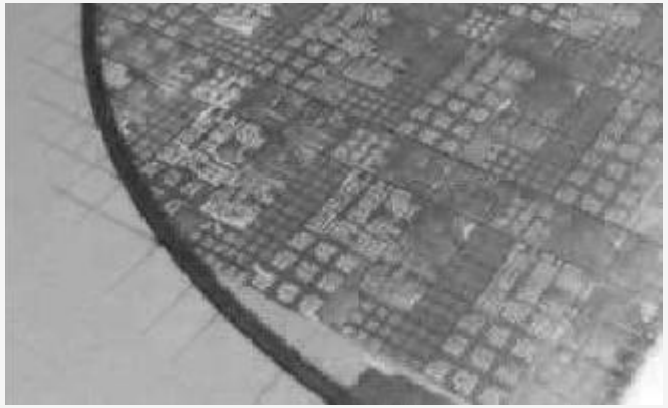
➔ 70µm diameter balls vs pillars and 20µm pillars results

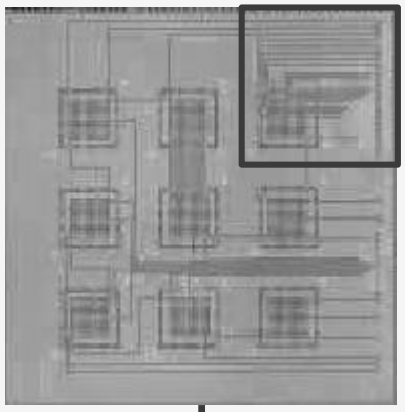
ZIBE TEST VEHICLES I

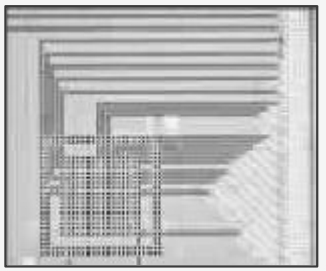
- Several test vehicles were designed & manufactured for qualification of stacking approaches
- Two routes for high density interconnects were evaluated
- Test vehicles feature design that permits electrical characterization

Test Vehicle	Bump Type	Bump Diameter	Bump Pitch	I/O Count	Stacking Process
TV 1	Cu-Pillar	20 µm	40 µm	3,870	TCB
					C2
TV 2	Cu-Pillar	30 µm	65 µm	2,295	TCB
					C2
TV 3	Cu-Pillar	40 µm	80 µm	1,287	C2
	Solder Balls				C4
TV 4	Cu-Pillar	70 µm	130 µm	567	C2
	Solder Balls				C4
TV 5	Solder Balls	130 µm	250 µm	135	C4

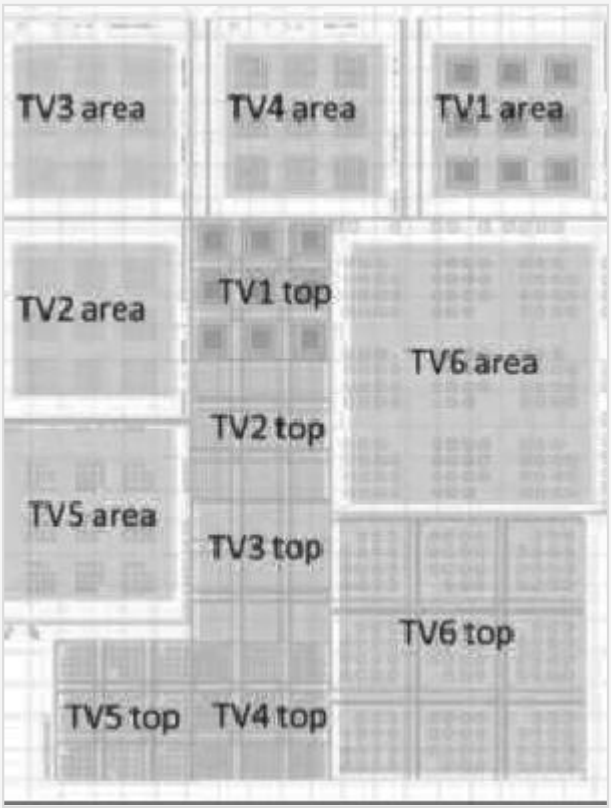
ZIBE TEST VEHICLES II

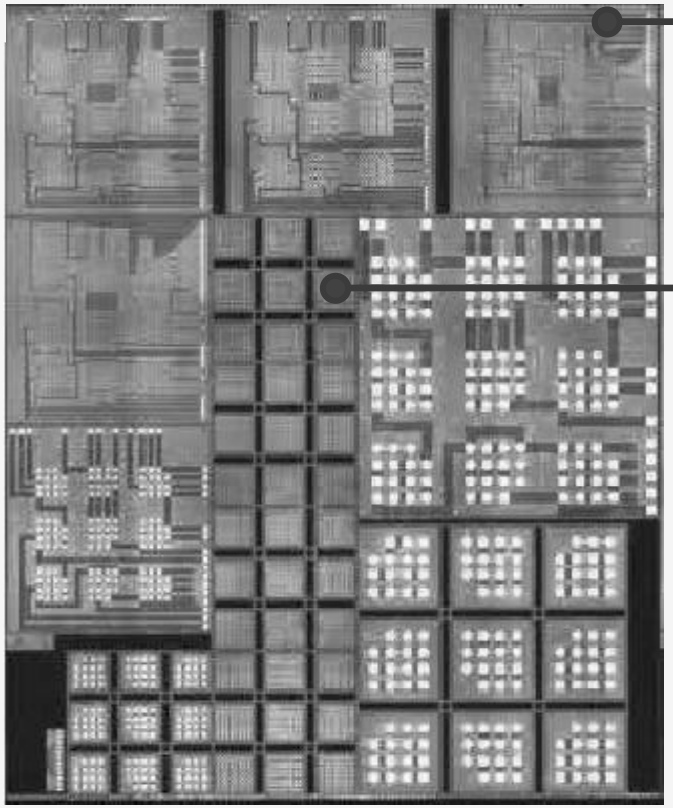


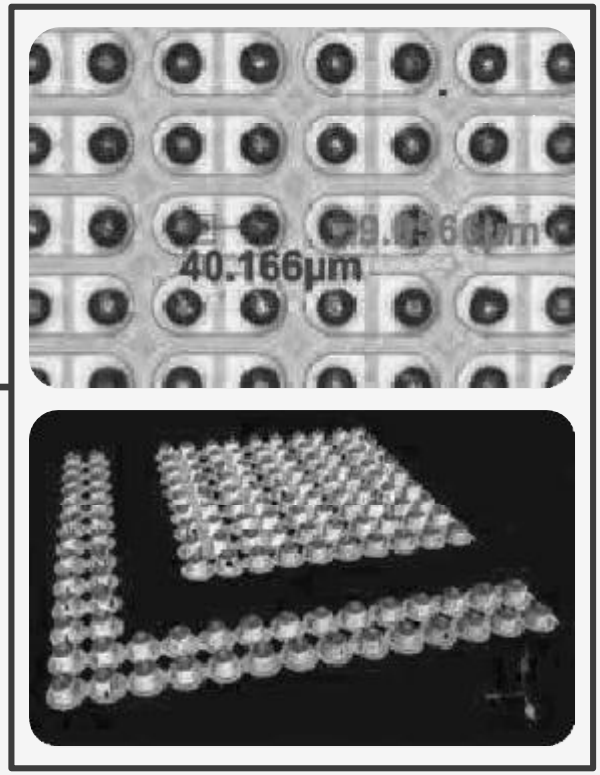




TV 1
Bottom die



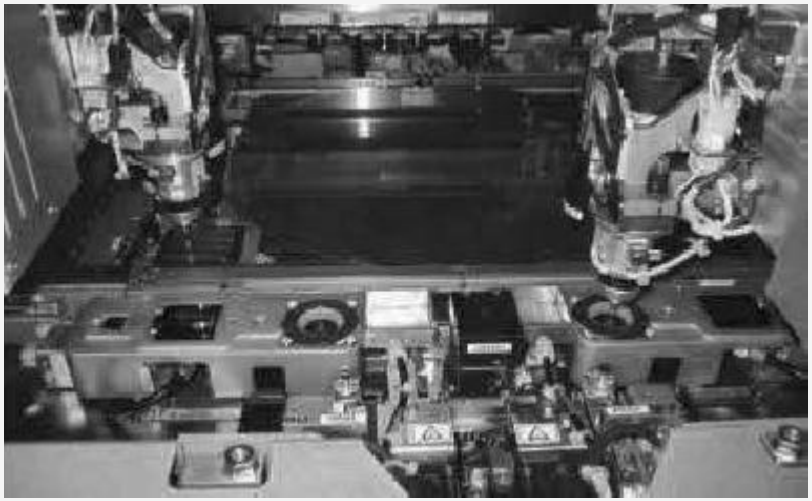


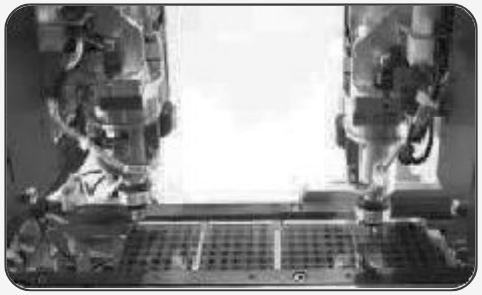


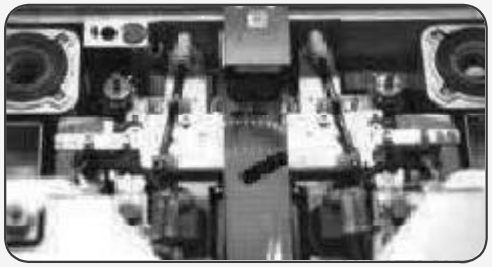
TV 1 – Top die

DIE BONDING EQUIPMENT

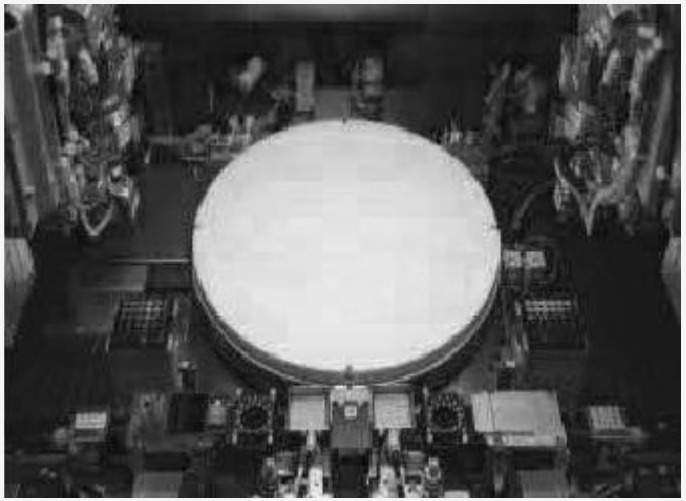
Machine configuration for **reflow processes** (e.g. C2, C4)

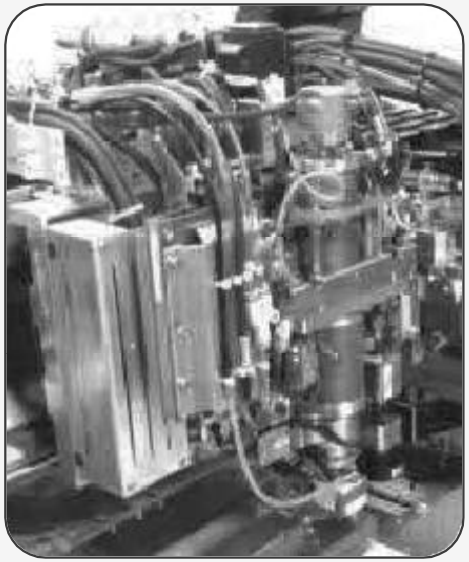




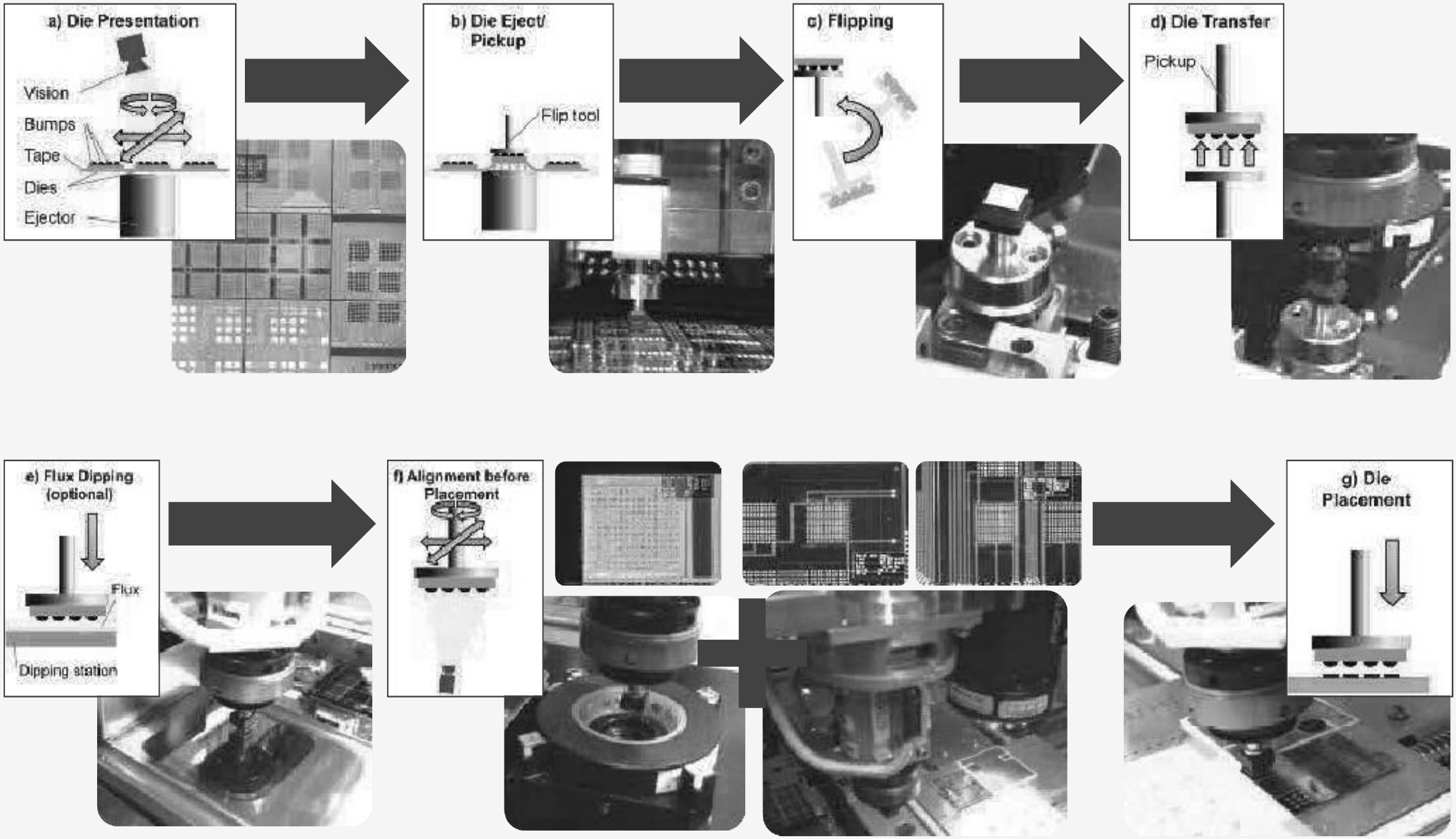


Machine configuration for the **TCB process**



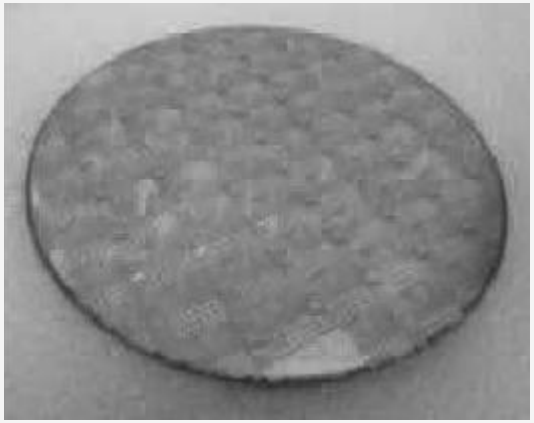


STACKING APPROACHES – PROCESS FLOWS (I)

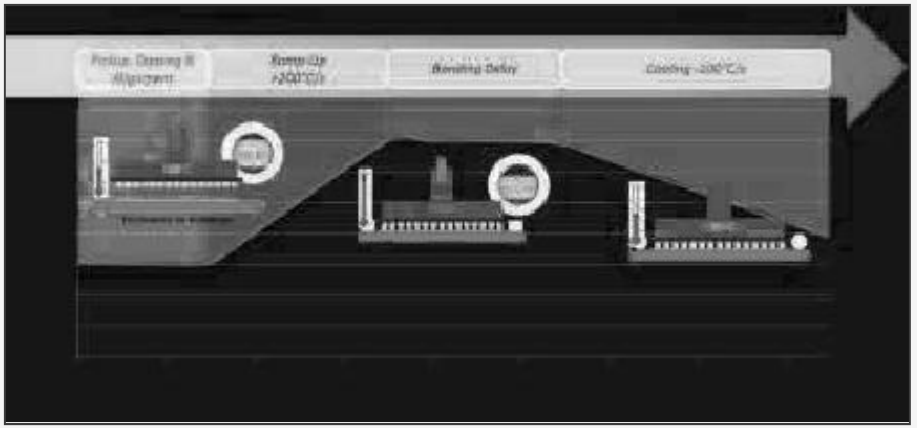


STACKING APPROACHES – PROCESS FLOWS (II)

Population of substrate wafer + solder reflow **(C2, C4)**

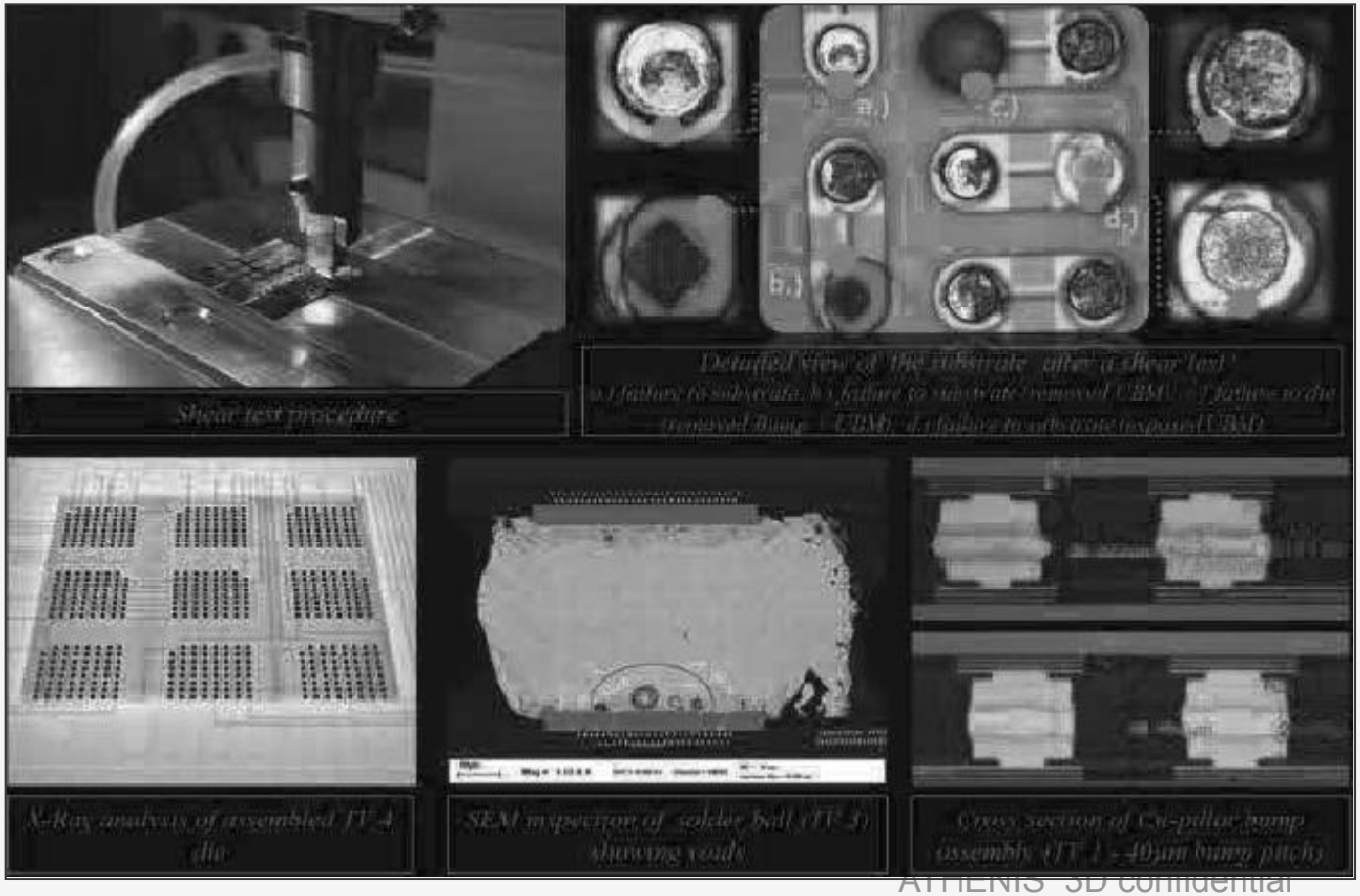


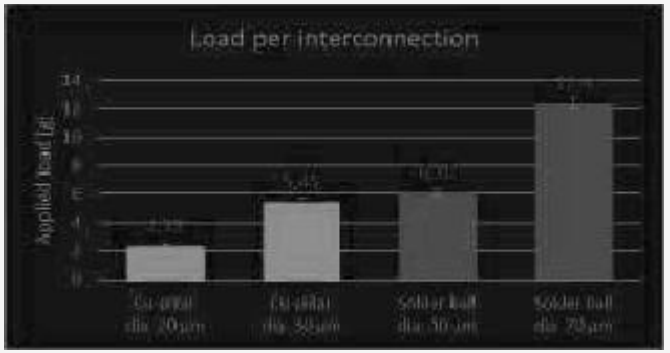
Local reflow **(TCB)**



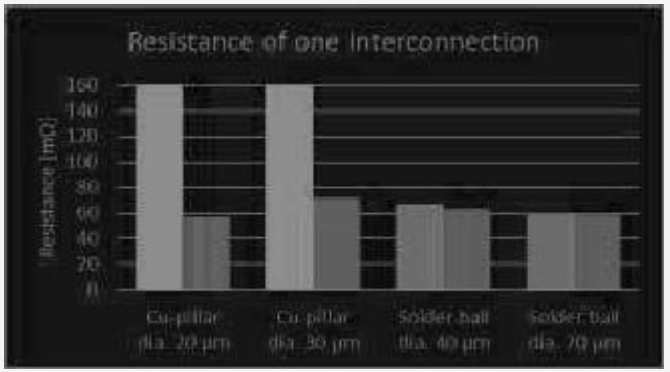
STACKING APPROACHES – ANALYSIS

- Tilt & bond-line thickness (BLT) – 3D Microscope
- Placement accuracy – X-ray microscope + cross sectioning
- Mechanical connection / joint strength / failure mode – Shear tests
- Electrical characterization





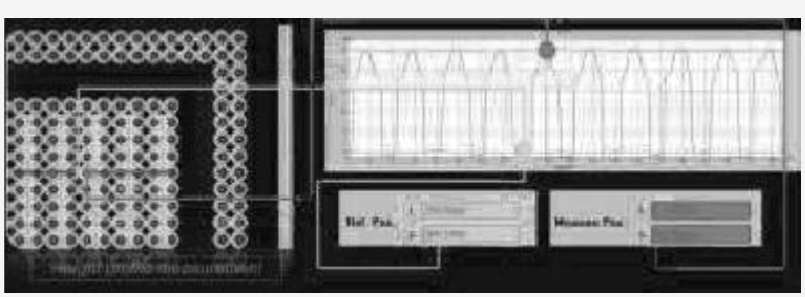
Shear test results

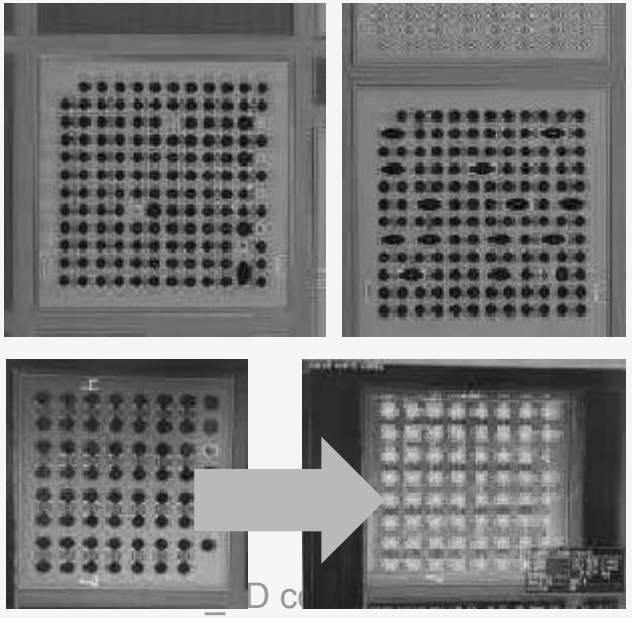


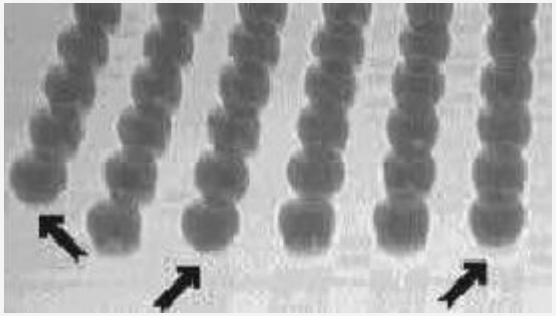
Electrical characterization

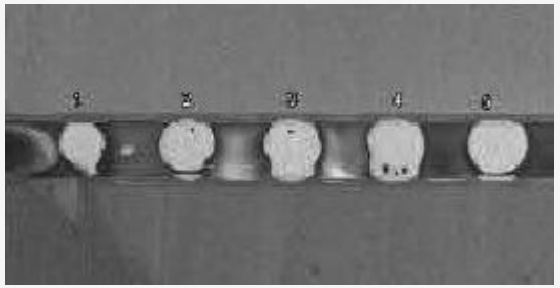
Results & Observations

- Accurate bonding realized due to placement accuracy of ±3μm@3s & ±5μm@3s for TCB and mass-reflow stacking approaches respectively.
- Tilt of ±1μm@3s and ±3μm@3s realized for TCB and mass-reflow stacking approaches respectively
- Resistance of electrical connection decreases w/ interconnection size
- Mechanical stability increases w/ interconnection size
- Cu-pillars showed high quality in contrast to solder balls









RESULTS & CONCLUSION

Results & Observations

- Accurate bonding realized due to placement accuracy of ±3µm@3s & ±5µm@3s for TCB and mass-reflow stacking approaches respectively.
- Tilt of ±1µm@3s and ±3µm@3s realized for TCB and mass-reflow stacking approaches respectively
- Resistance of electrical connection decreases w/ interconnection size
- Mechanical stability increases w/ interconnection size
- Cu-pillars showed high quality in contrast to solder balls

Conclusion

- C4 process recommended for bump pitches down to 100µm
- C2 process recommended for bump pitches down to 40µm (for C2W-applications)
- TCB process recommended for ultra-fine pitch applications (bump pitch <50µm)
- Higher throughput can be realized w/ mass reflow process, whereas the TCB-approach is more suitable for high-end applications

T4.4 TSV and WLP process module simulation [Leader: FhG]

Start: M4, 20.03.2014

End: M32, 20.07.2016

Schematic of the integration technology. The parts considered for simulations are highlighted.

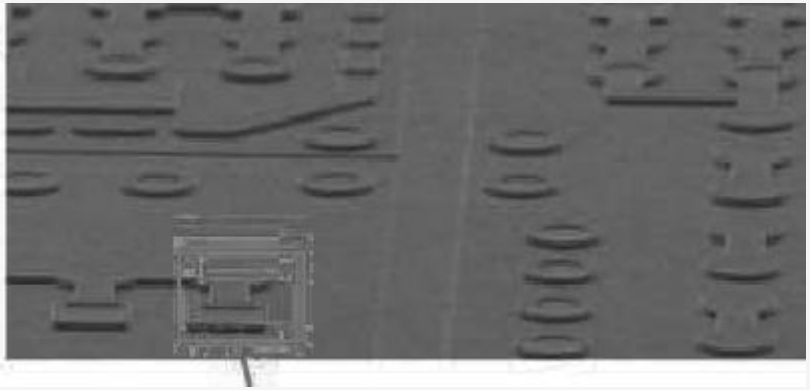
Objectives:

Using inputs (materials, properties, technology geometry) from T4.1 to T4.3 and perform Electrical, Thermal and Mechanical (ETM) simulation to assist process development including:

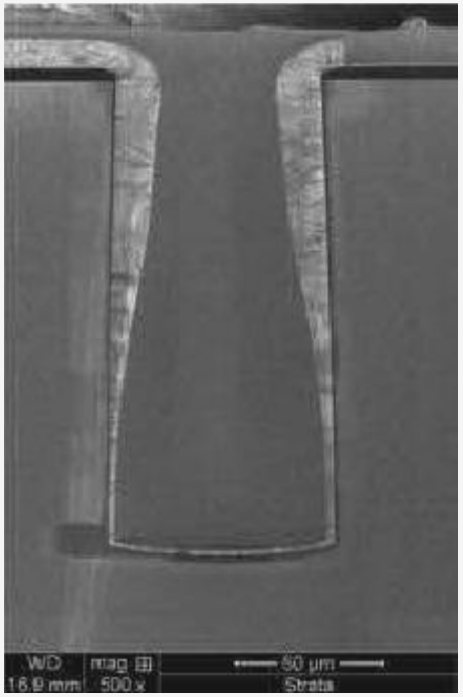
- Micro scale ETM stress distribution
- Macro scale ETM stress distribution
- Reliability issues identification (weaknesses to thermal cycling or hot spot during operation)

T4.4 – TSV and WLP process module simulation

- Thermo-mechanical simulations of TSVs and the back-side RDL to support technology development
- Simulation provides insight into strains and stresses which are not accessible experimentally
- Investigation of different passivation structures
- Simulations performed with ANSYS

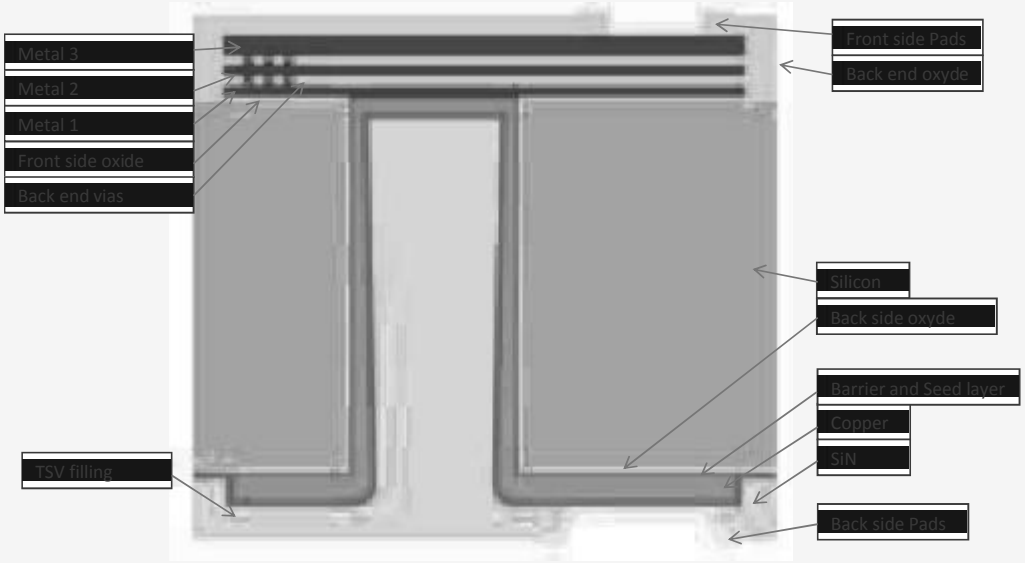


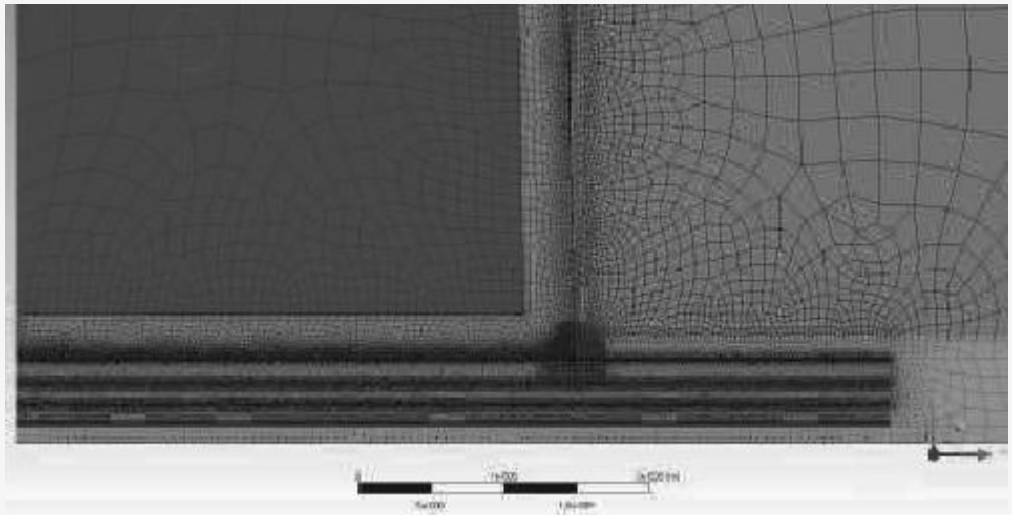
Backside RDL

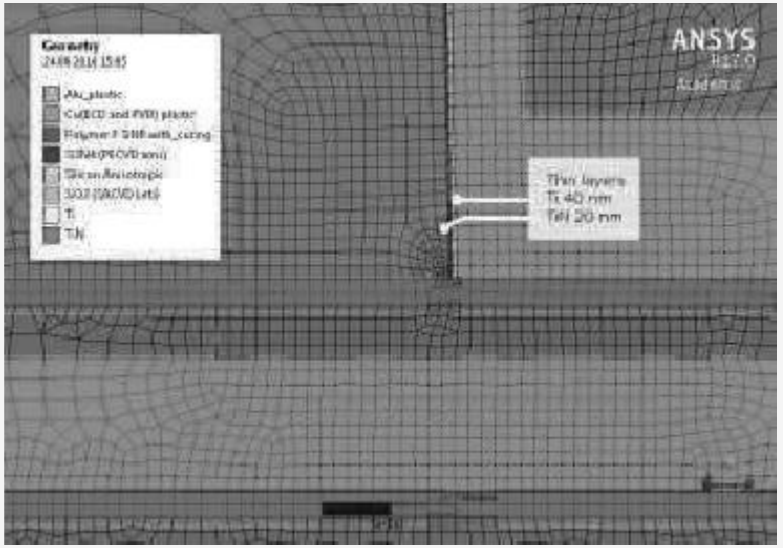


T4.4 – TSV and WLP process module simulation

- Numerically challenging due to the high ratio of problem size (200 µm) and the thickness of the thinnest layers (20 nm)

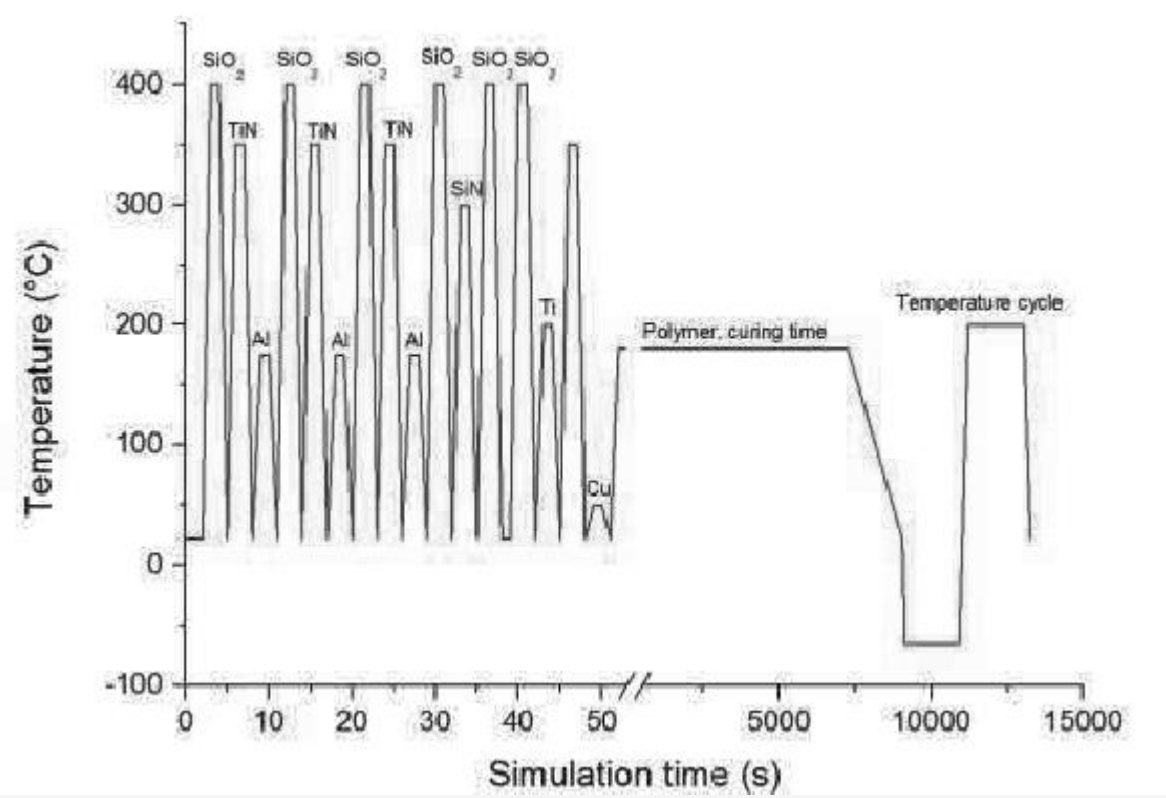






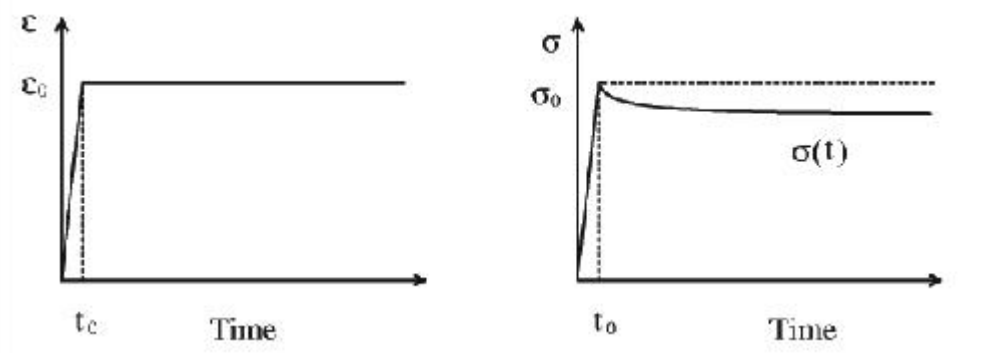
T4.4 – TSV and WLP process module simulation

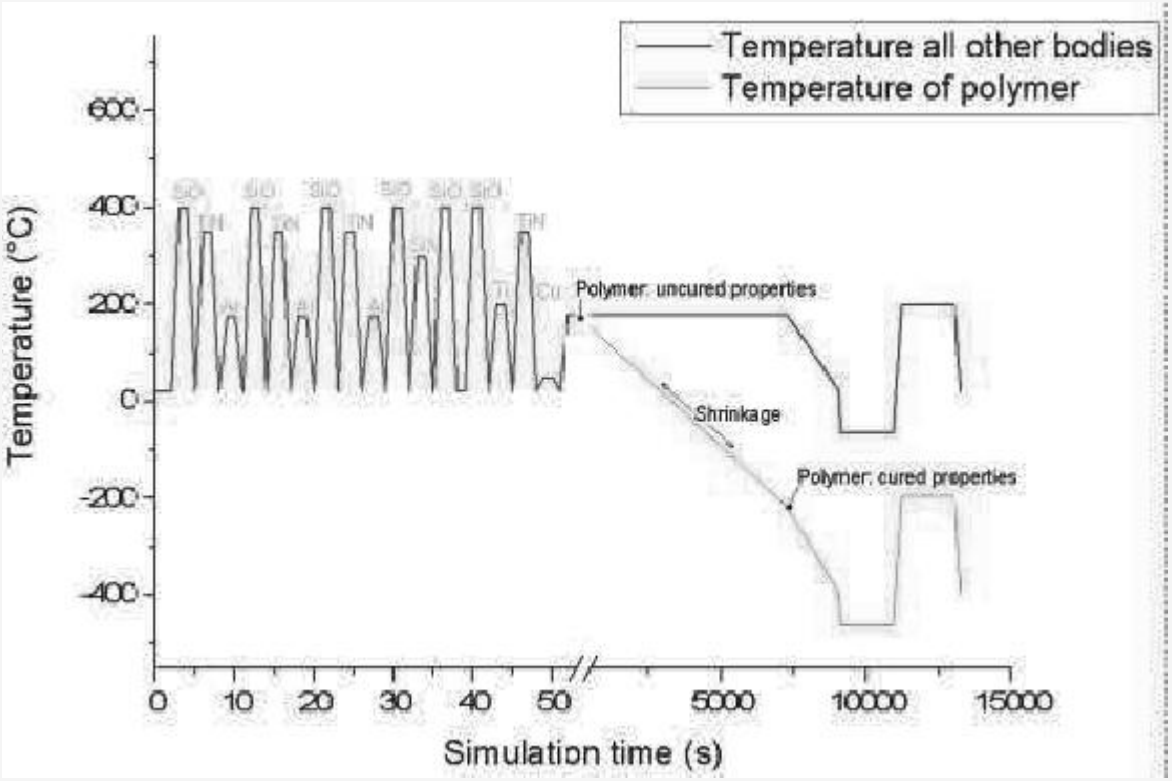
- Simulation of the complete fabrication process and the following cycling to include intrinsic strains in a realistic way
- Metals and dielectrics assumed to show elastic or plastic behavior
- Intrinsic strain taken into considerations via the deposition temperature (corresponds not necessarily to the physical deposition temperature)
- Polymer curing required transient simulations



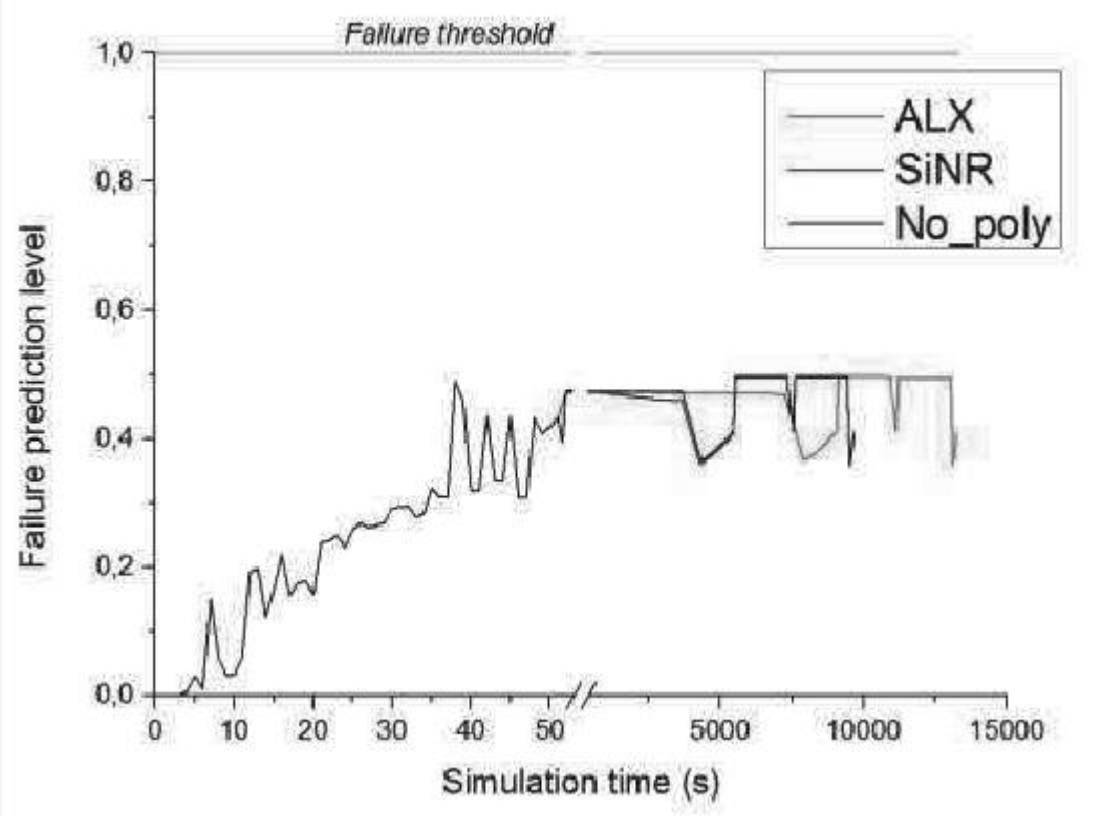
T4.4 – TSV and WLP process module simulation

- Polymers assumed to show viscoelastic behavior
- During curing, Young's modulus, retardation times and the viscosity change by a factor of 5
- Change of materials parameters and a 10% shrinkage implemented via an artificial temperature change for the polymers only

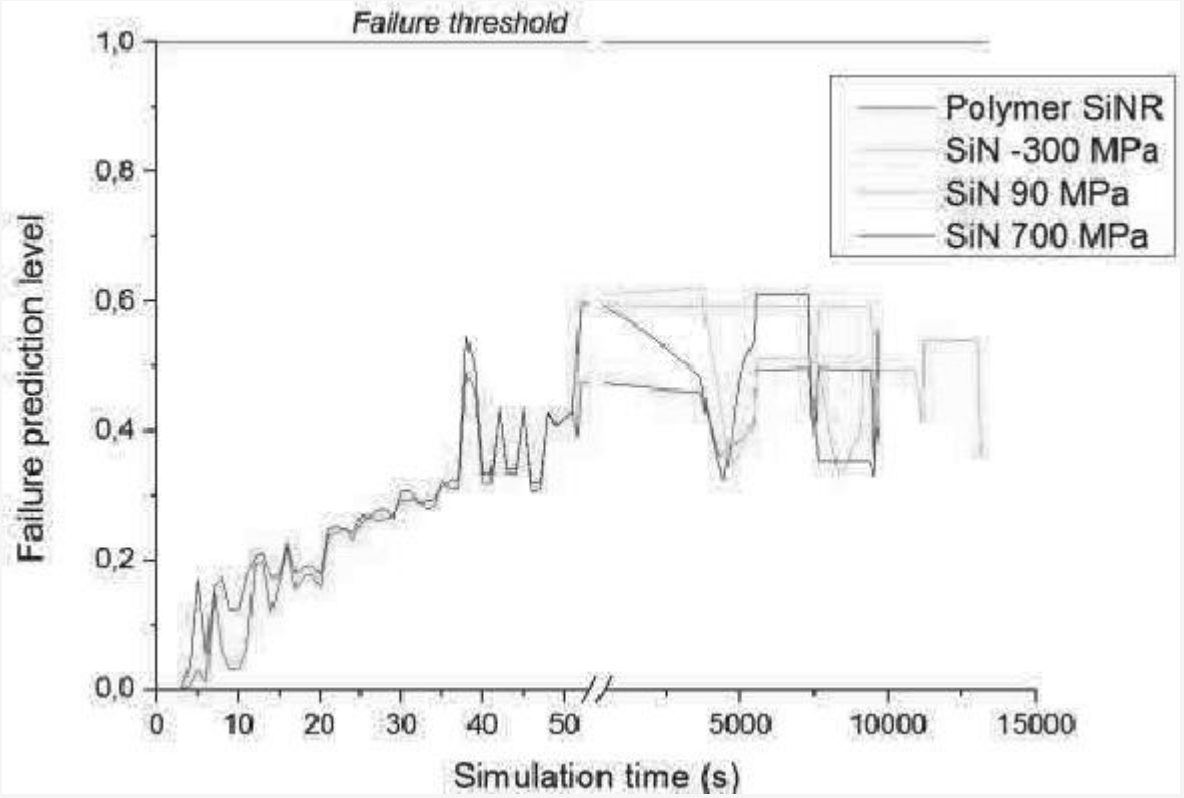




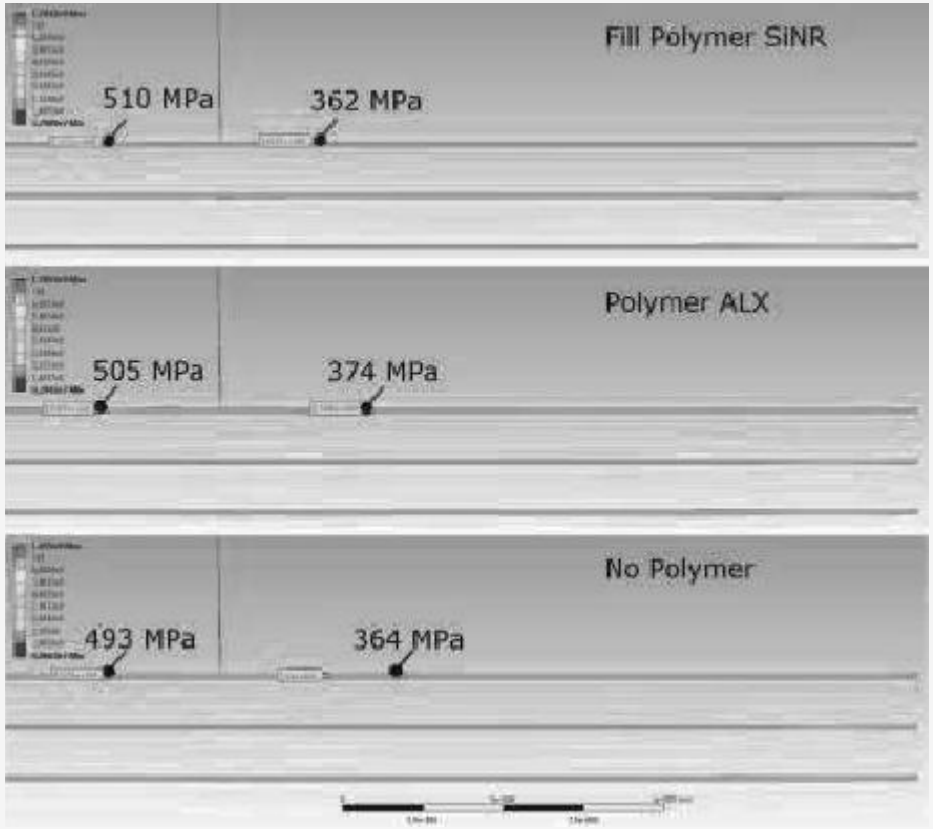
- No significant influence of polymers (SiNR and ALX polymers) found on the silicon dioxide layers

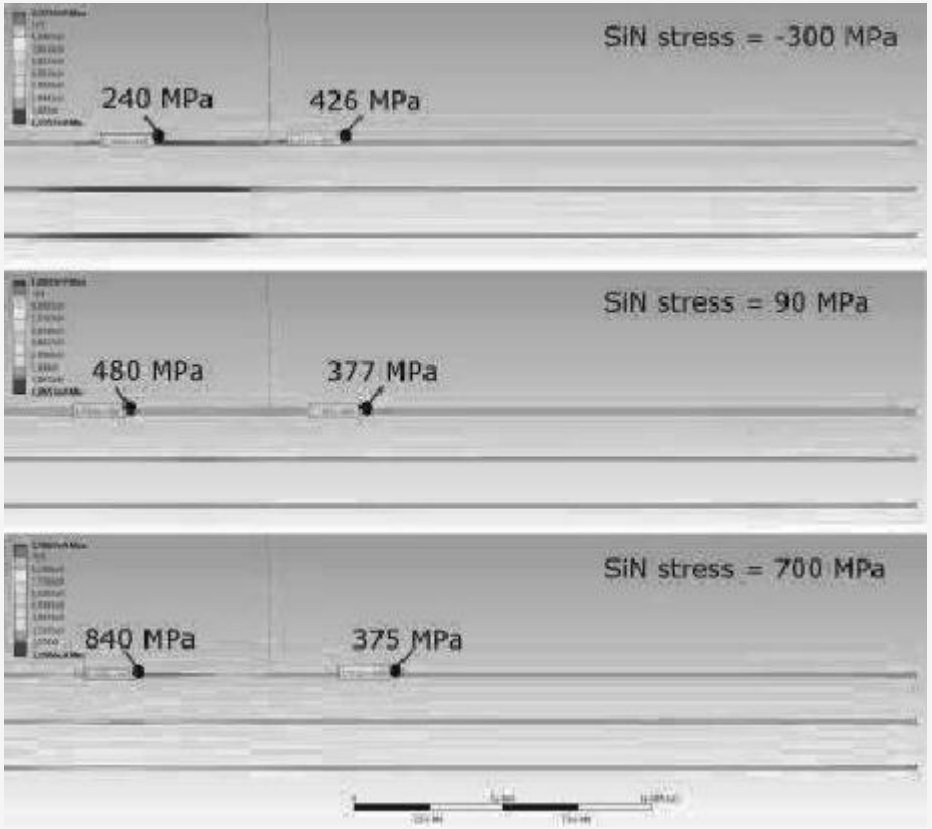


- A 1 µm SiN passivation layer led to higher stresses in the oxide layers but still no failure of the oxides was predicted



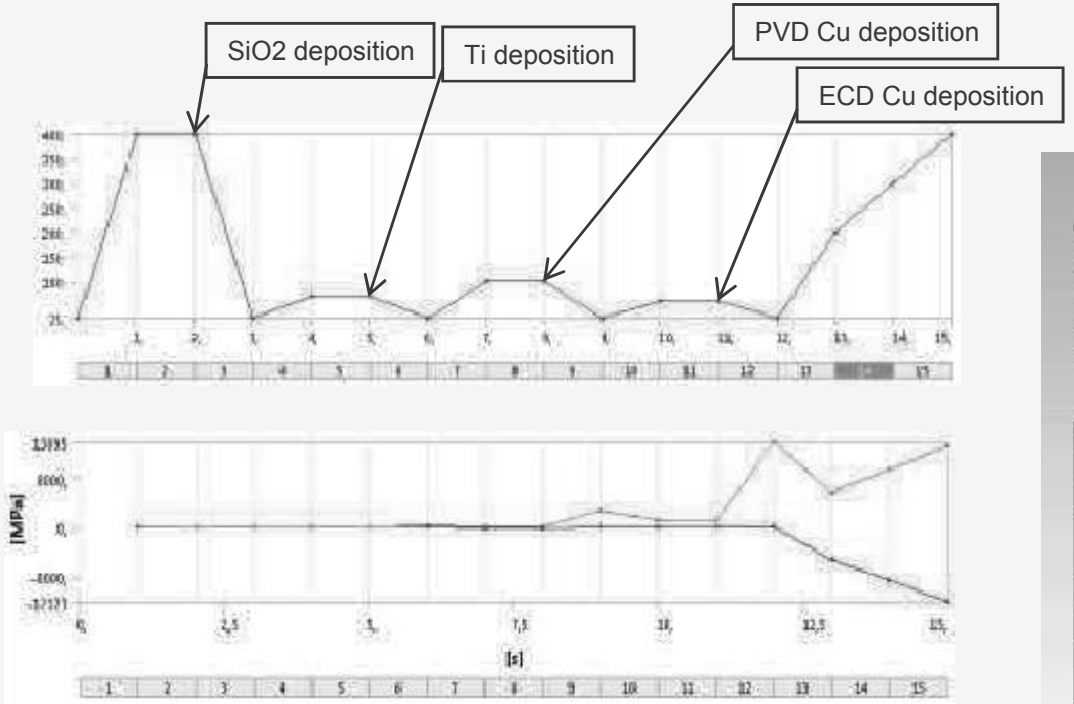
- Significant influence of the SiN passivation on van-Mises stresses in the TiN layer (90 MPa SiN layers give a more homogeneous distribution than without passivation)



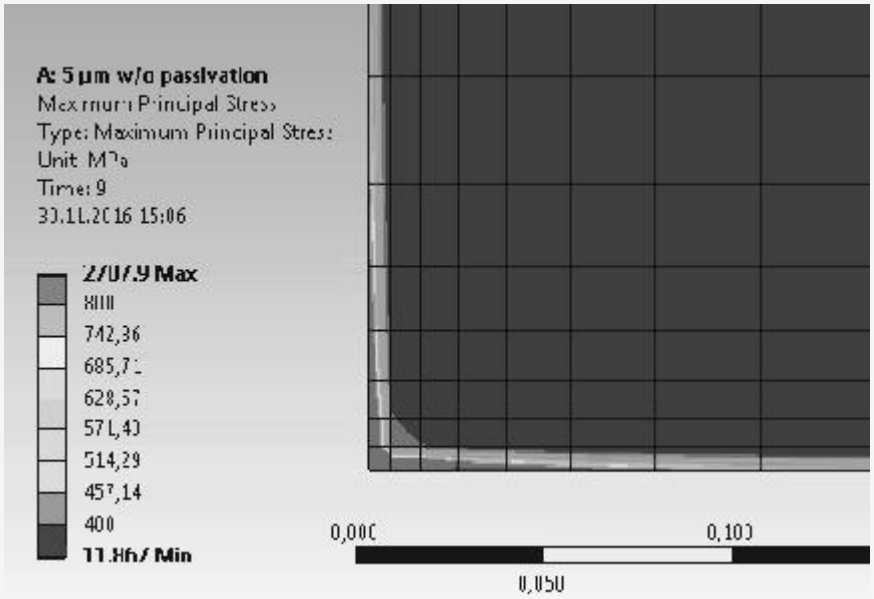


T4.4 – TSV and WLP process module simulation

- Additional RDL simulations in Fall 2017 to include changes in the structure
- Tensile stress (positive) exceeding the yield stress found during some fabrication and cycling steps
- Better knowledge of corner geometry would be needed for better prediction



Example: Thick copper RDL



Electromigration Induced in Open TSVs

Electromigration reliability issue in open copper TSV

Void initiation

- Where voids are nucleating?
- Times needed to nucleate a stable void (t_I)

Void evolution

- Growing void
- TSV resistance increase
- Time to reach resistance failure criterion (t_M)

Numerical methods

- Finite element solution of model equations in COMSOL
- Application of Diffuse Interface model to describe evolving void surface

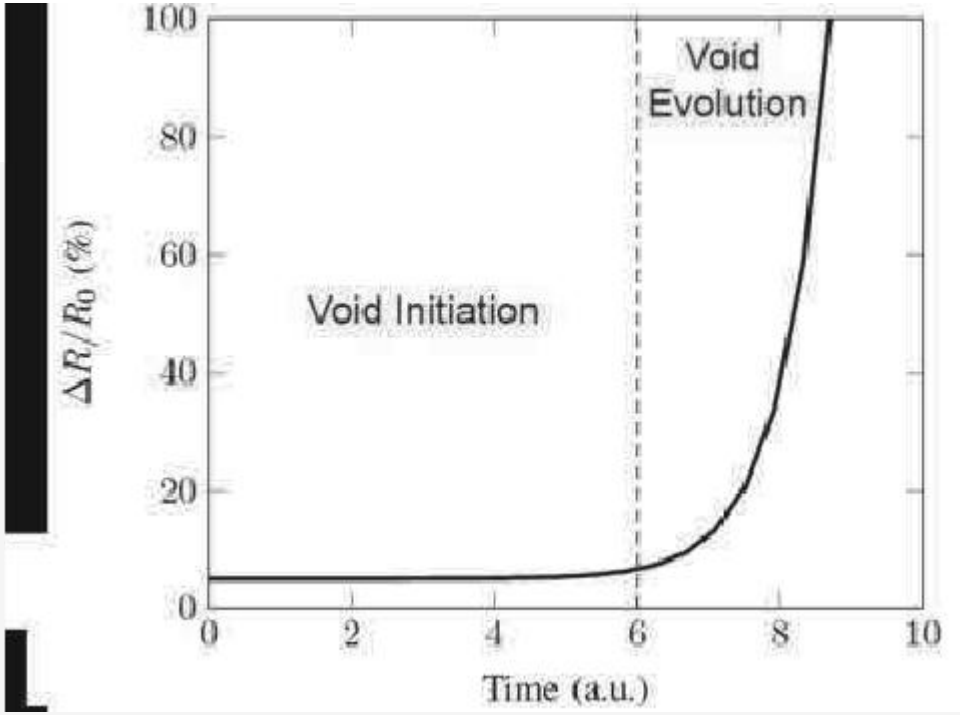
Verification

- Comparison with Black's equation prediction

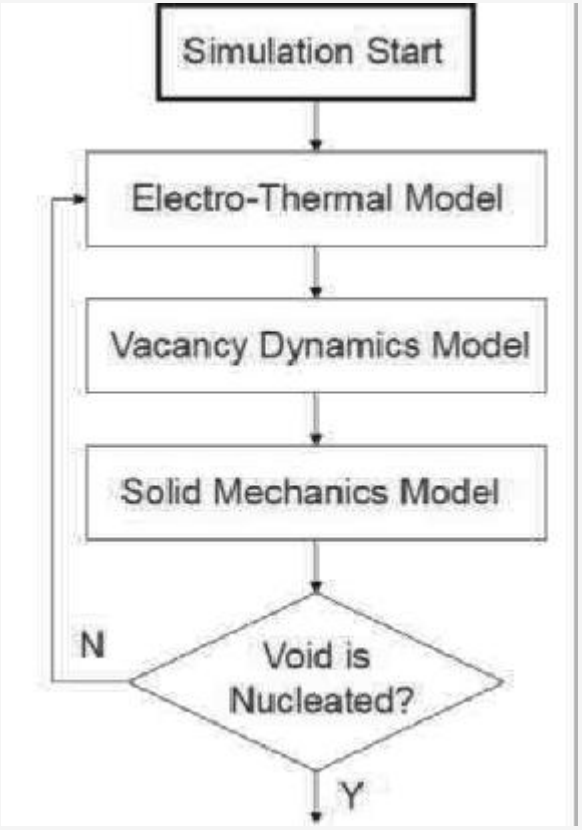
Electromigration: Time to Failure (TTF)

Two phases of the electromigration failure development

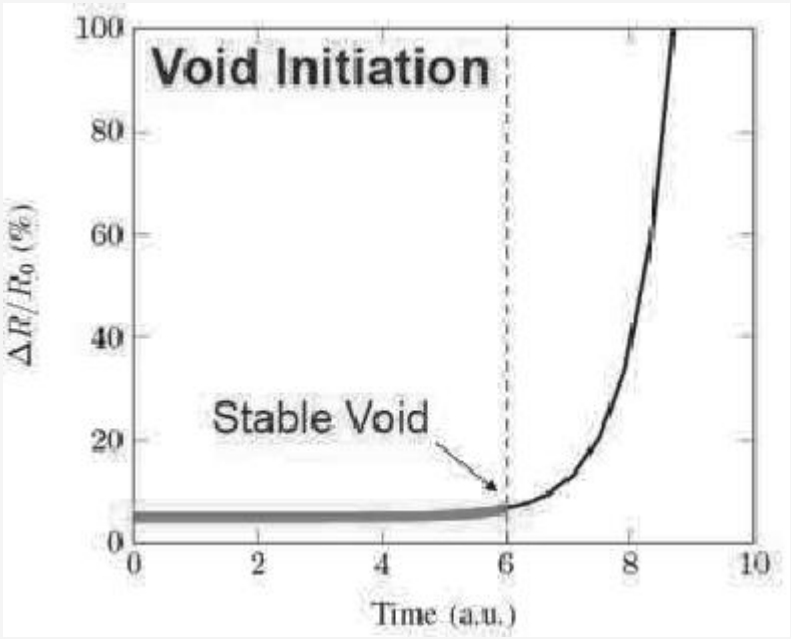
$$t_{TTF} = t_I + t_N$$



Electromigration: Void Initiation

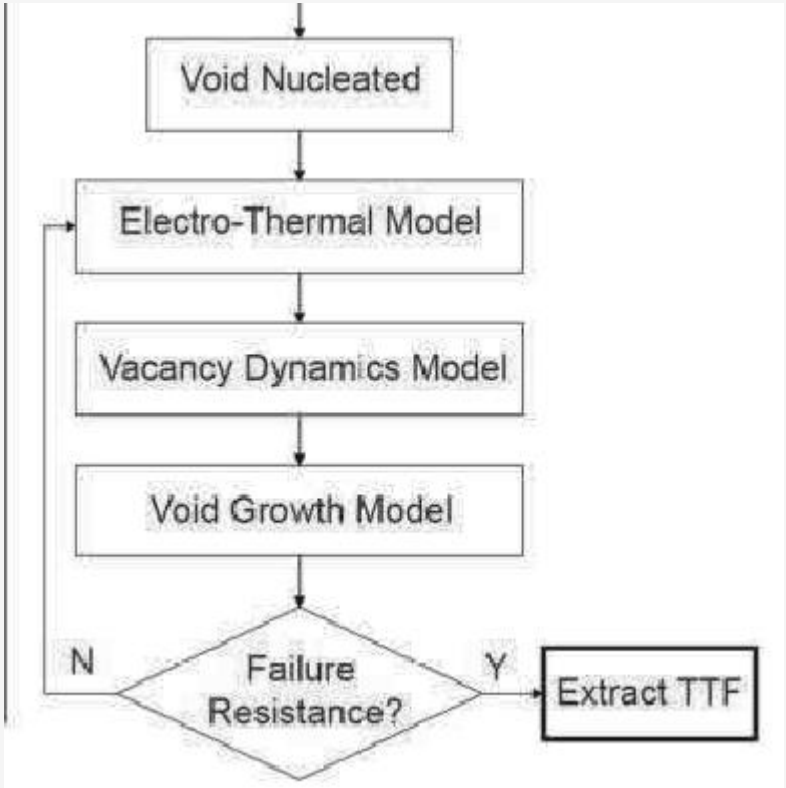


$$t_f \sim \frac{1}{j^2}$$

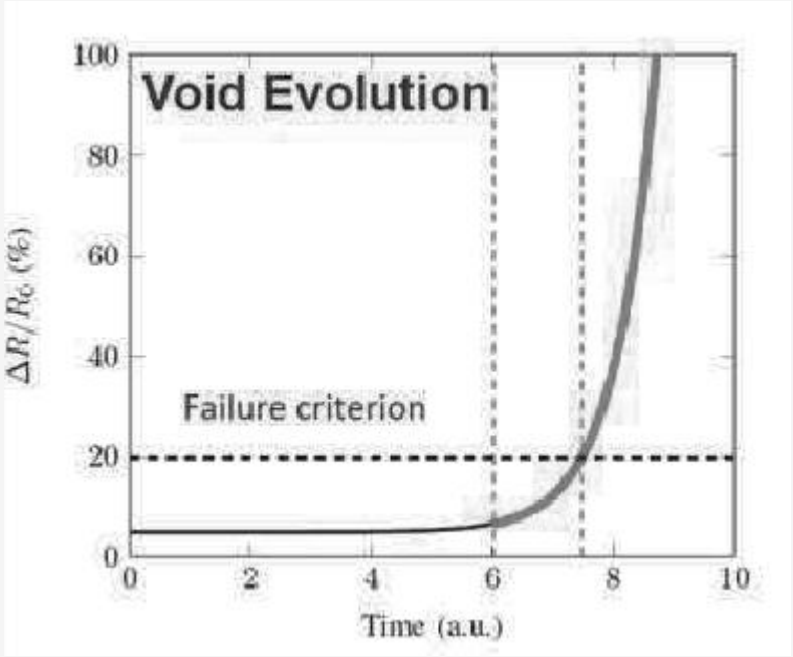


Ceric *et al*., IEEE TDMR, vol. 9, 2009,
Ceric *et al*., Mat. Sci. Eng. R, vol. 71, 2011

Electromigration: Void Evolution

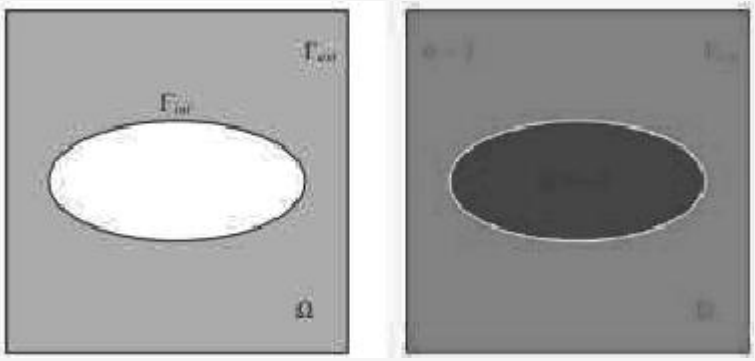


$$t_N \sim \frac{1}{j}$$



Fridline and Bower, JAP, vol. 85, 1999
Ceric *et al*., IEICE Tran. Elect. vol 86, 2003,
Lacerda de Orio, PhD thesis, TU Wien, 2005

Electromigration: Diffuse Interface Model

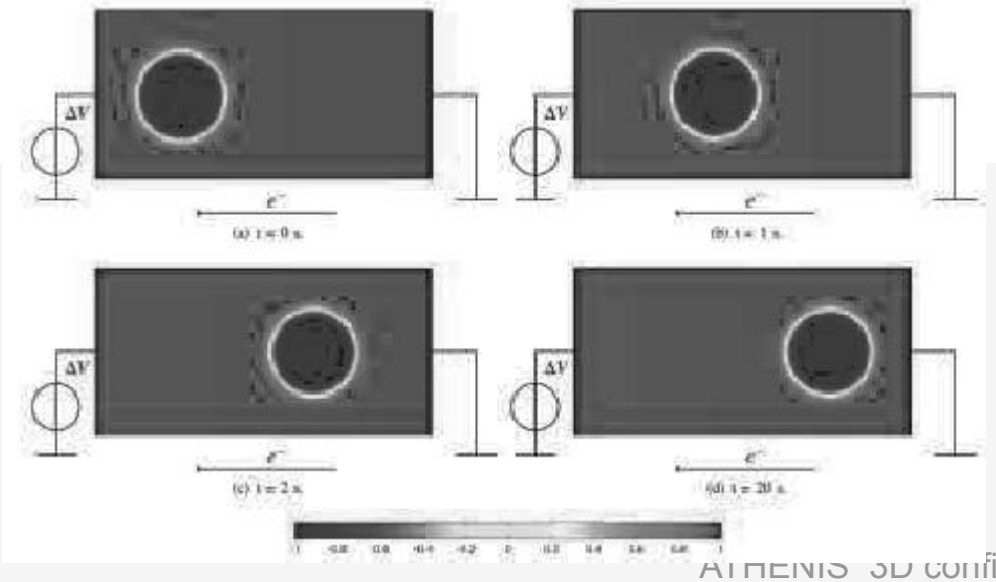


Sharp interface Diffuse interface

Diffuse interface

Metal/void surface described by numerical order parameter ϕ

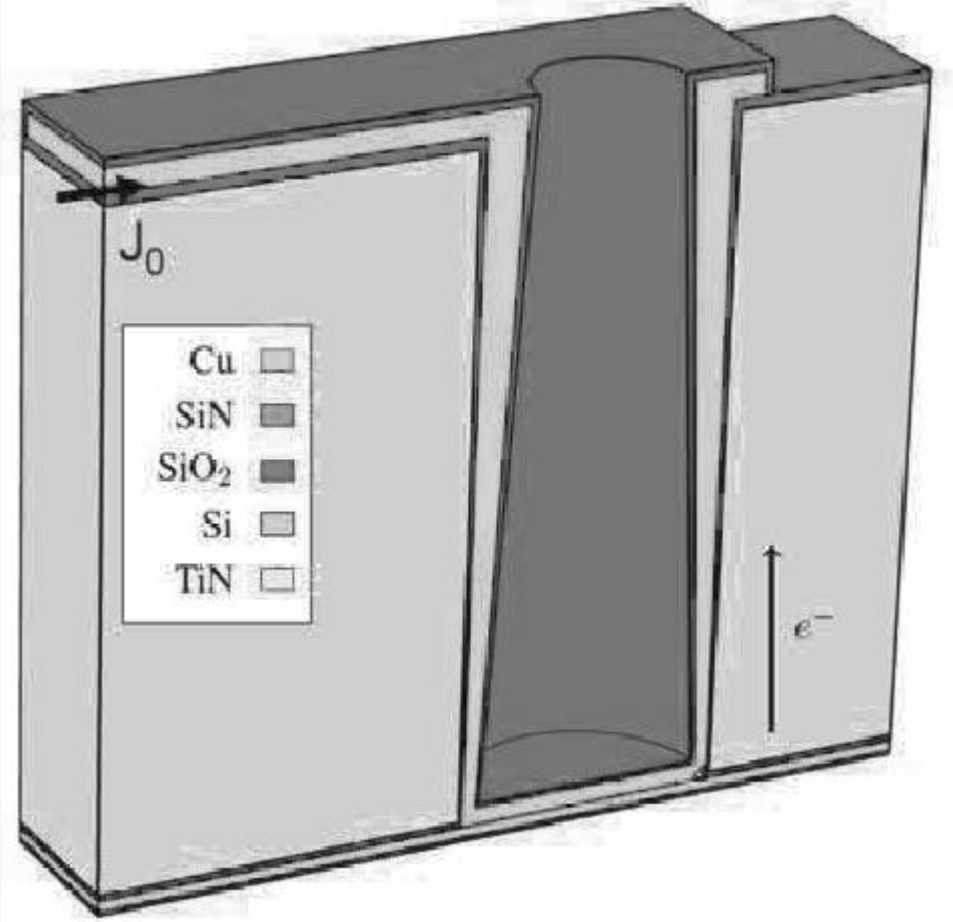
Dynamics of order parameter distribution determined by electromigration



Example: Void driven by electromigration in linear interconnect

Studied Case: Electromigration Voiding in TSV

TSV Top



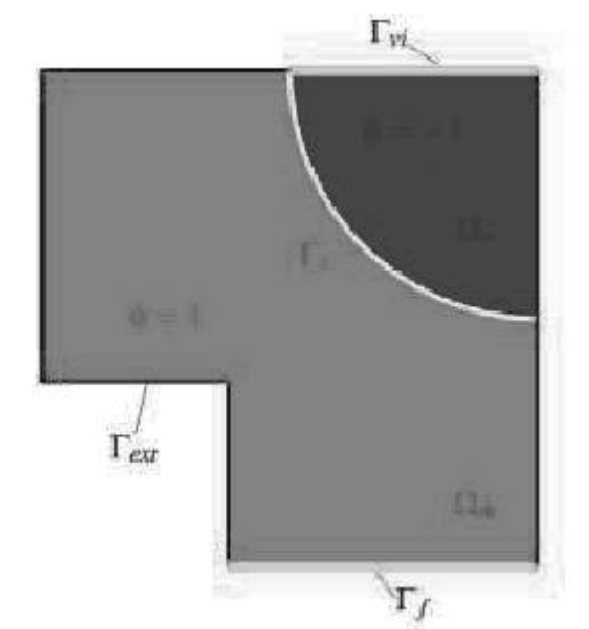
TSV Bottom

Test conditions
- $T = 200°C$
- $J_0 = 1MA/cm^2$

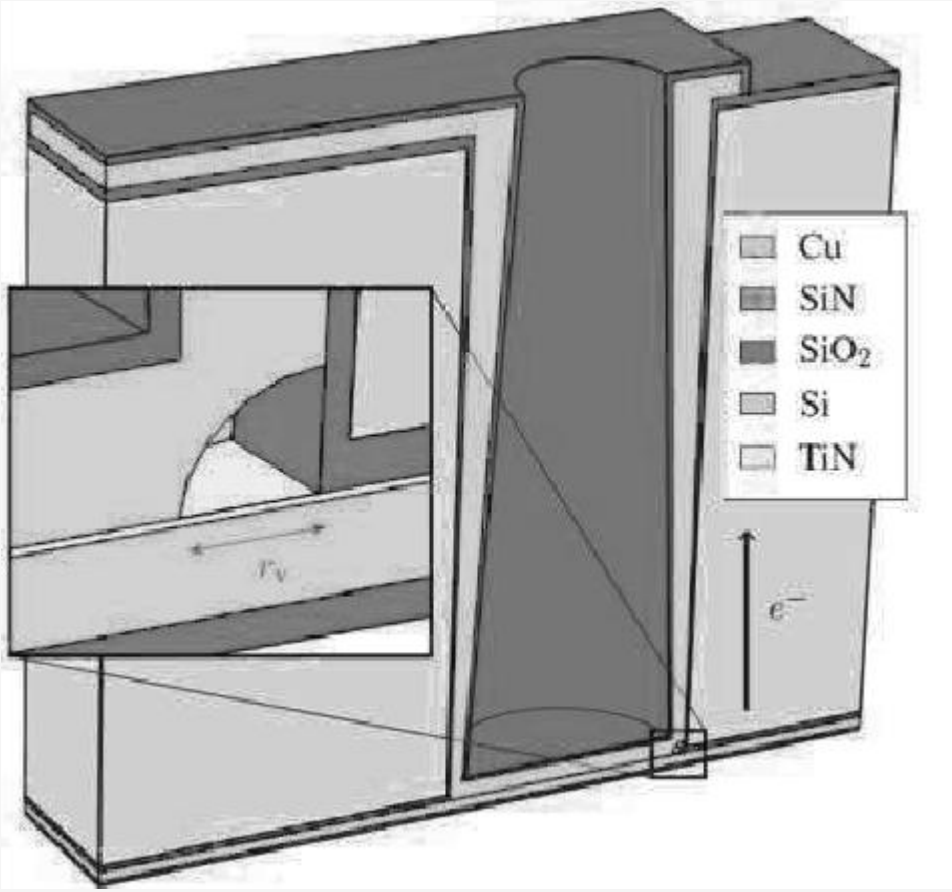
Boundary conditions
- Thermal insulation
- Fixed mechanical constraints
- Electrical insulation
- Electromigration blocking Cu/TiN

Rovitto *et al*. ECTC 2016, ,
Rovitto *et al*. submitted Microel. Real.

Studied Case: Electromigration Voiding in TSV

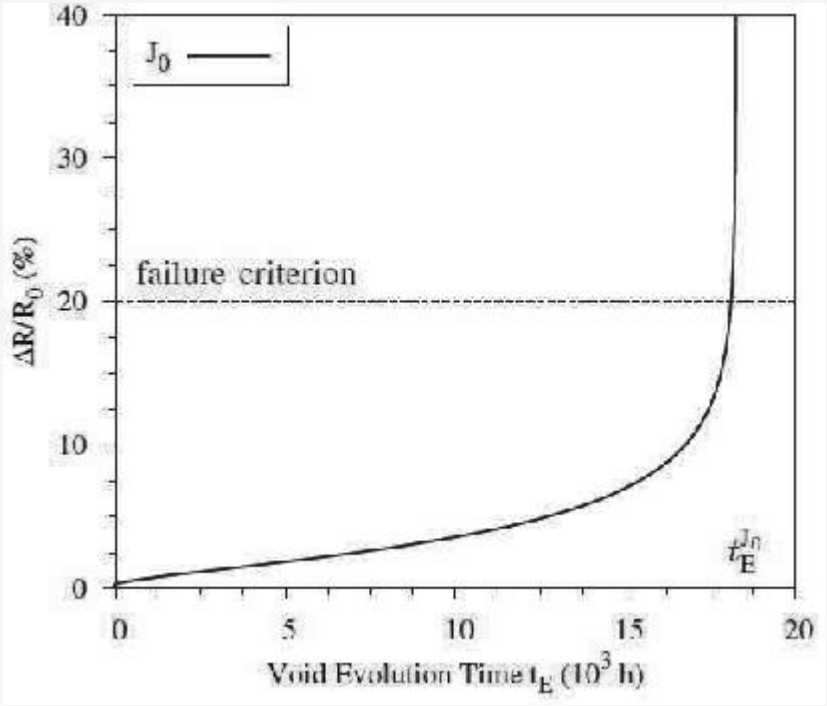


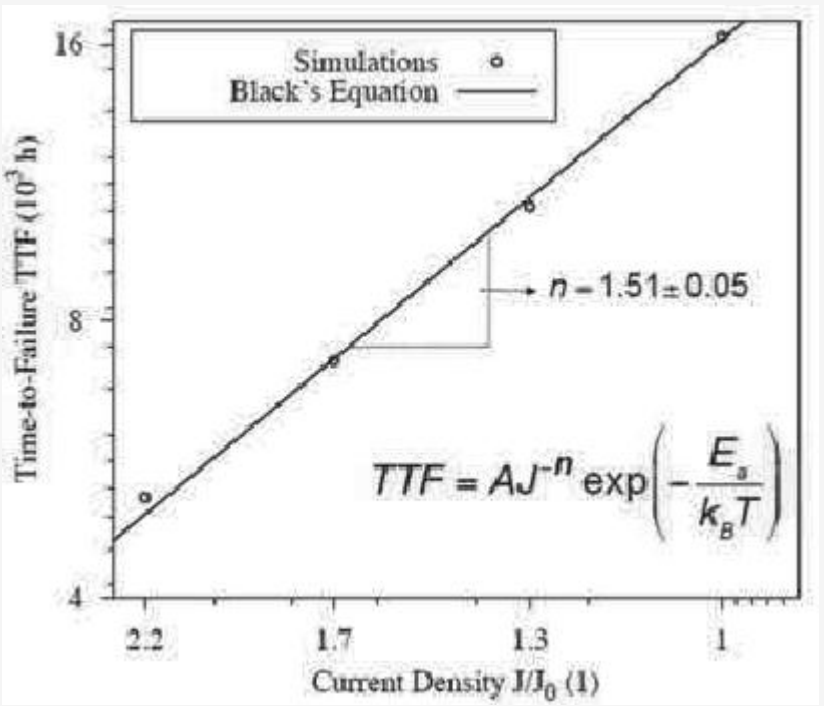
Diffuse interface void description



Void placed in the TSV structure

Conclusions: Comparison to Black's Equation





Conclusions

Two-phases electromigration model used as the basis for simulation
Void evolution described by the Diffuse Interface model
Simulations were carried out for different applied current densities
Predicted TTFs correspond to the values obtained by Black's equation

WP4: Task 4.5 Overview

T4.5 Wafer level overmolding (WLOM) process Development for automotive requirements [Leader: CEA Leti]

Start: M30, 04.2016

End: M36, 10.2016

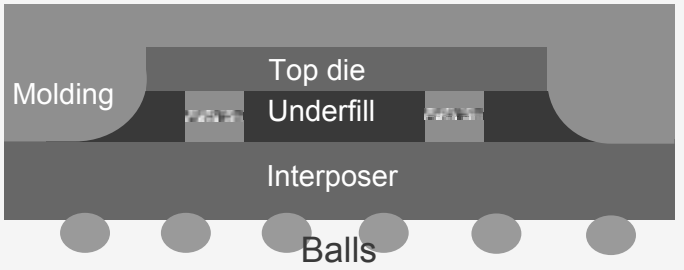
Harsh conditions ➔ Molding and underfill are required!

WLOM :

- **→Permits high mechanical protection of the interconnections/pillars (Encapsulation)**
- **→Limits the stress**
- **→Ensures planarization**

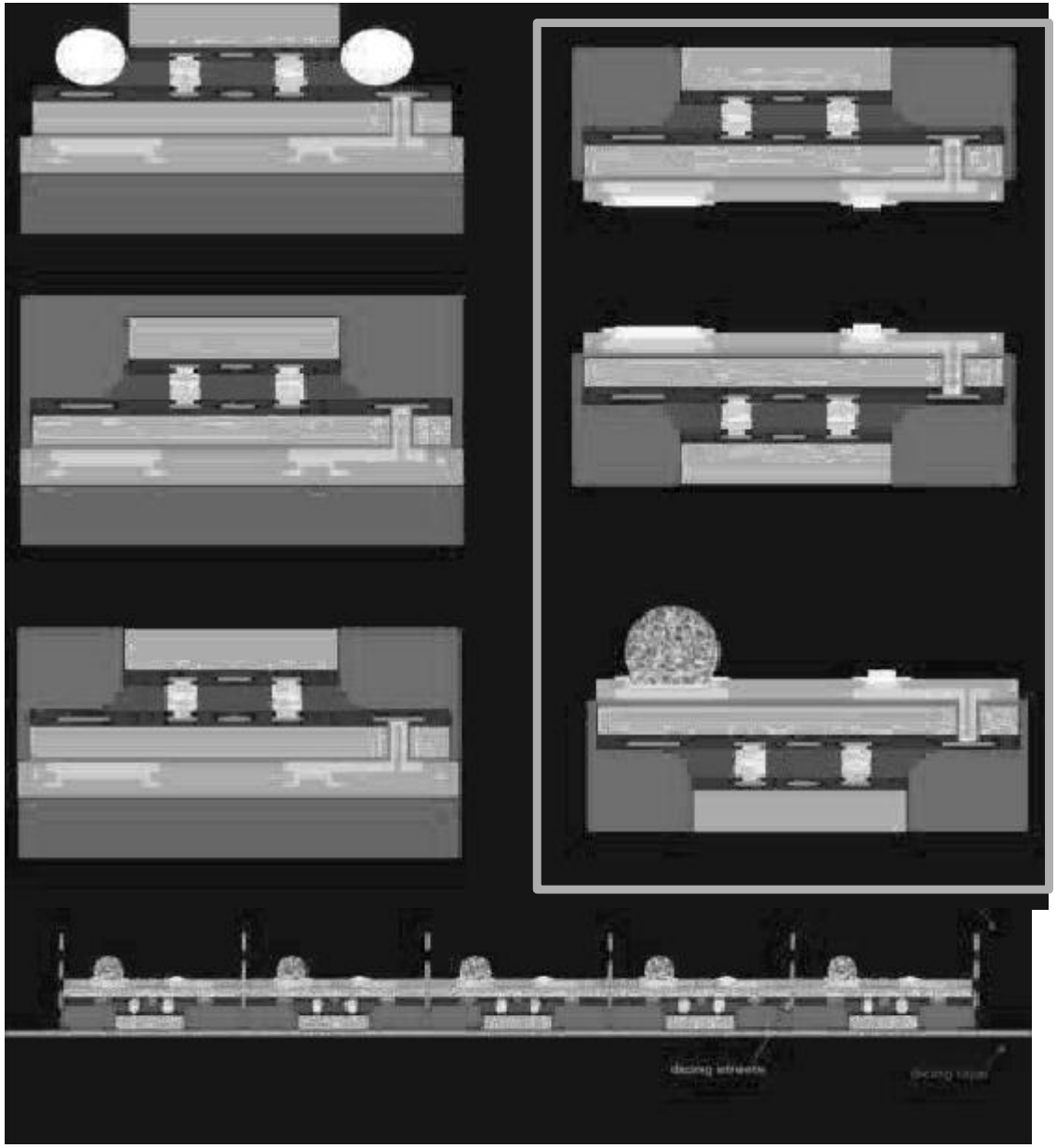
Screen printing:

- **→Permits the balling/bumping at wafer level**
- **→Is a cheap & easy technique for further mounting process on application board**



Schematic cross section of WLP device (top and bottom die, copper bumps/pillars interconnection) with WLOM process

Stacking Process flow: with molding ➔ WLCSP



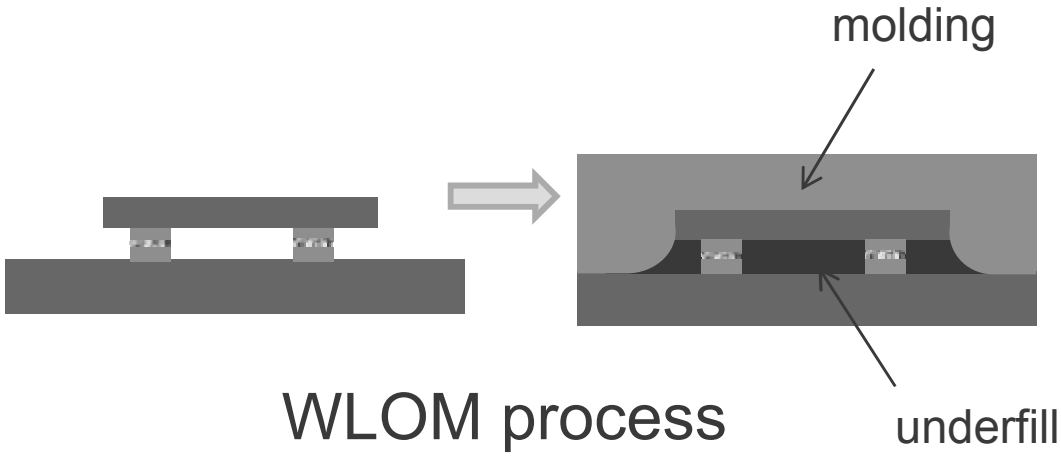
Simplification of the process flow for handling

Usually complex process steps due to thin wafer handling (warp, detection, silicon breakage)

From debonding to dicing process (step 4 to 7), a 600µm to 700µm thick is easy to handle!

WP4.5: WLOM introduction

Leti is equipped with a dry film lamination tool to deposit the over molding material



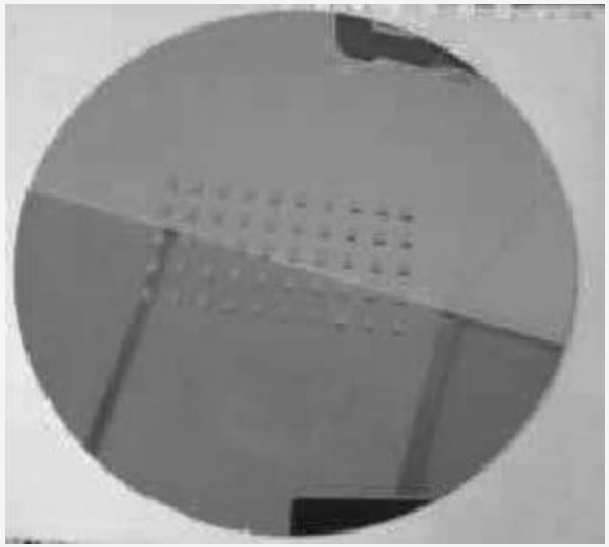
WLOM process

Takatori laminator (Team 300)

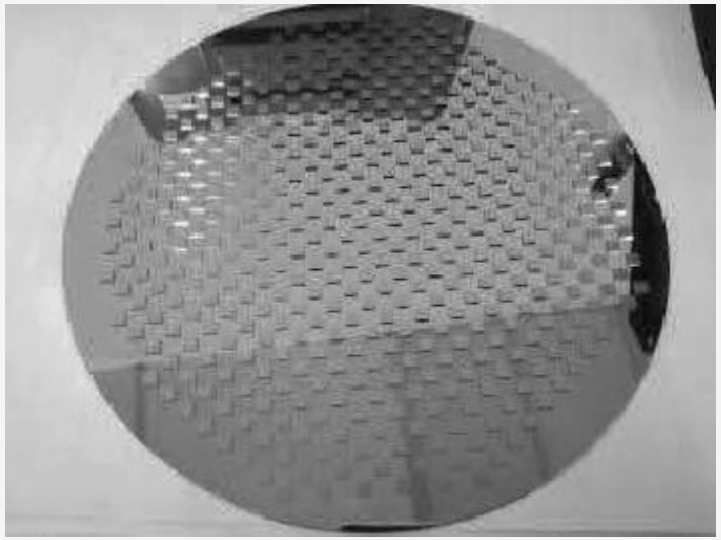
- The dry film is laminated on the wafer with a top roll
- The top chuck applies the dry film on the wafer with a pressure
- The chamber is under vacuum
- The film is then cured to allow the flow of the polymer in the interstices
- Capability to perform underfilling and molding in a single process step

VEHICLE TESTS PRESENTATION

- The top dies dimensions as been defined to be equal as 4 WAT1 top dies
- 2 mappings:
  - A partially populated design (50 top dies in the center)
  - A half populated design: Top dies are in staggered rows



Partially populated design

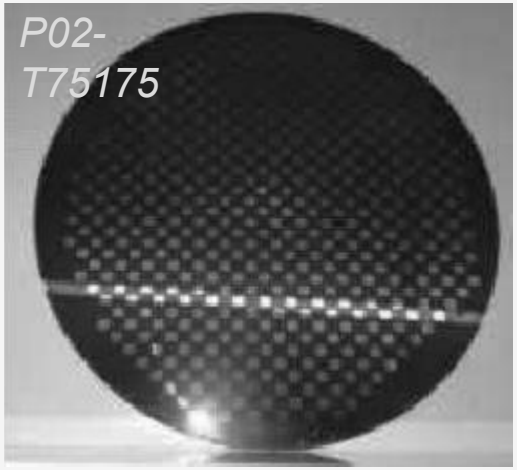


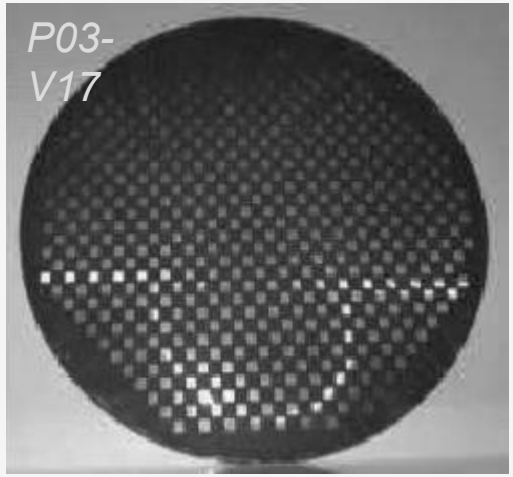
Half populated design

- From the 2 mappings, the impact on the warpage of the number of reported top dies will be studied.

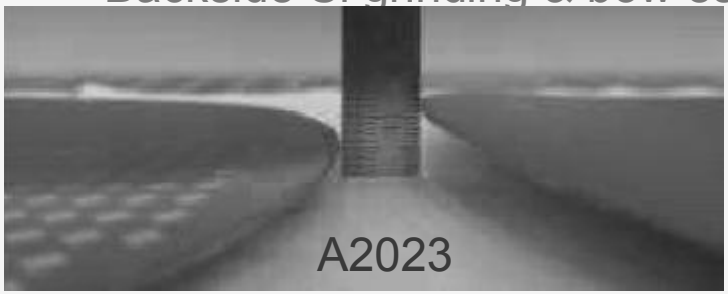
MOLDING GRIDING & BACKSIDE SI GRINDING: BOW MEASUREMENT

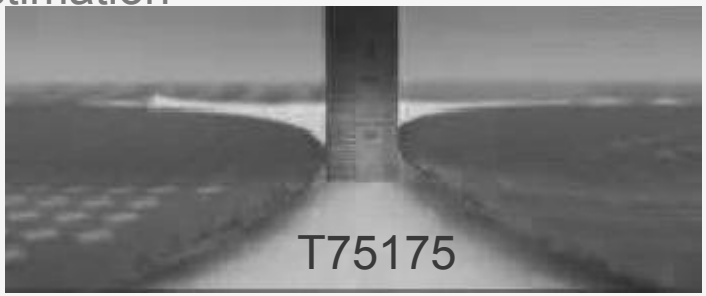
- Molding grinding

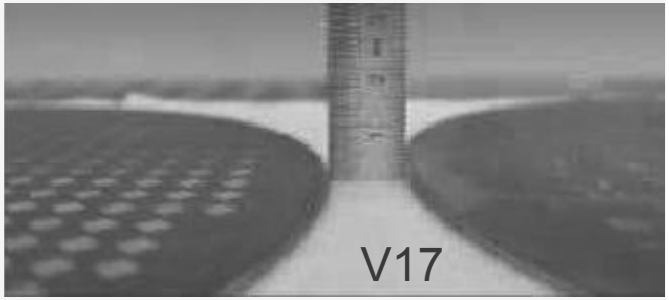




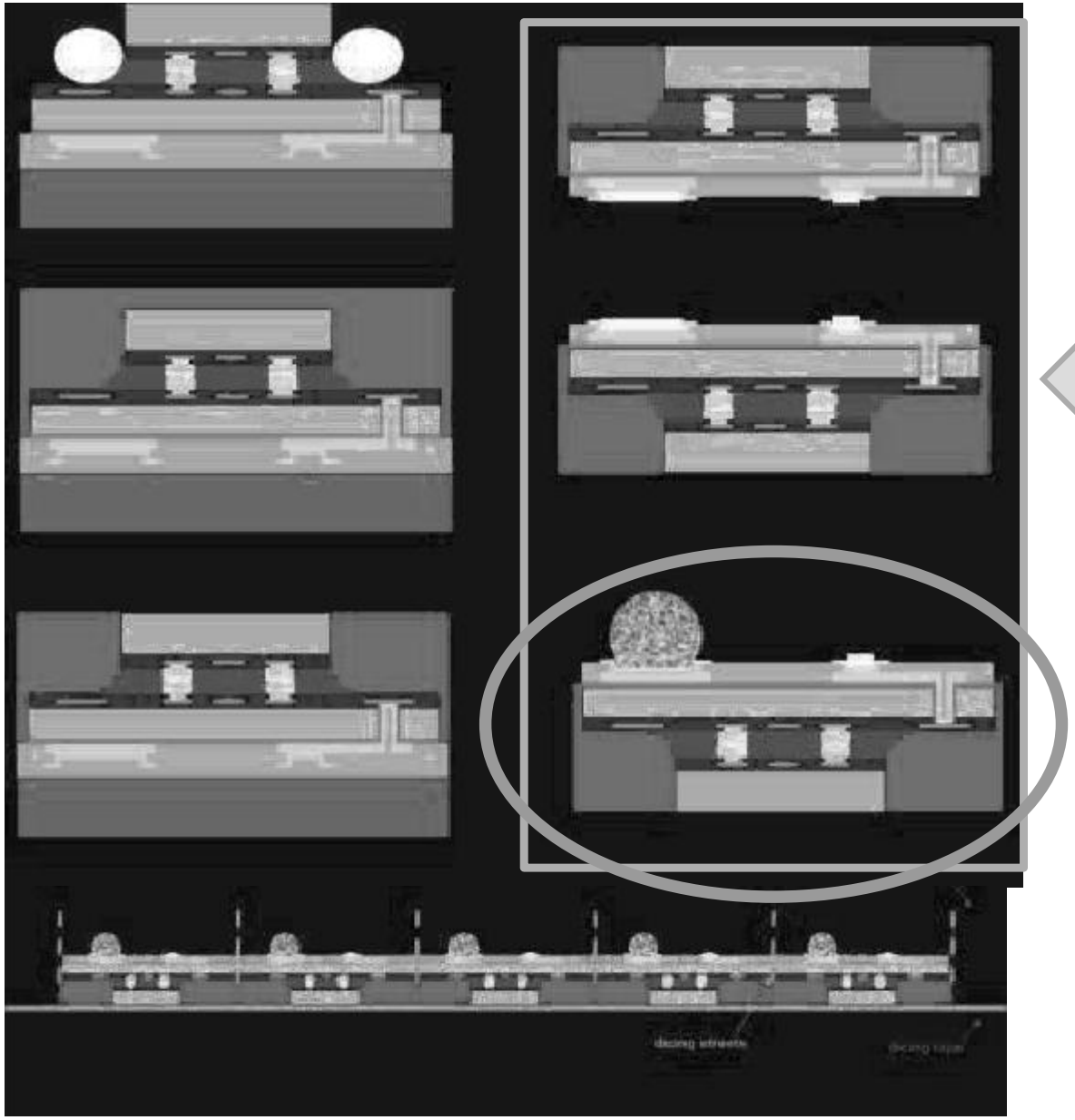
- Backside Si grinding & bow estimation







Stacking Process flow: with molding ➔ WLCSP



Simplification of the process flow for handling

Usually complex process steps due to thin wafer handling (warp, detection, silicon breakage)

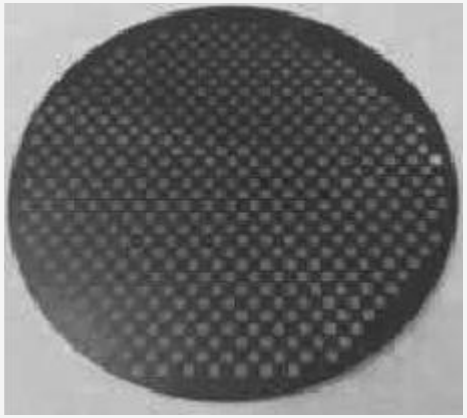
From debonding to dicing process (step 4 to 7), a 600µm to 700µm thick is easy to handle!

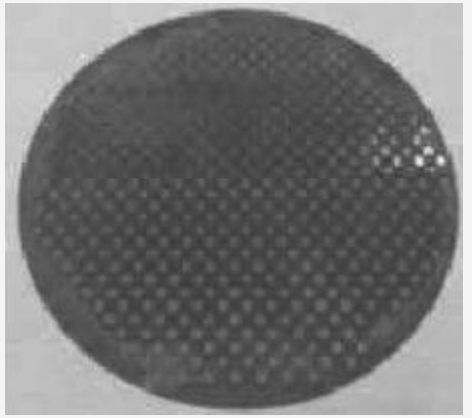
FINAL RESULT → PROCESS VALIDATION!

Nagase T751

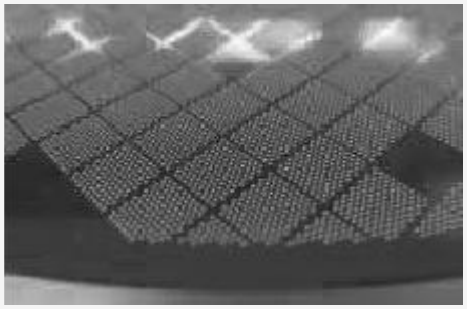
ShinEtsu SiNR V17

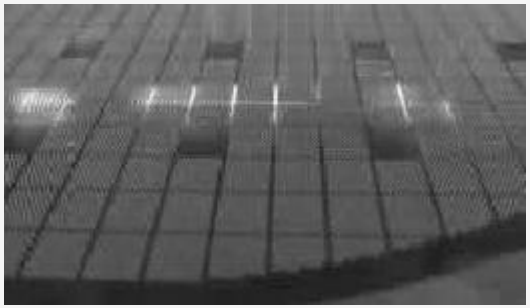
- Front side





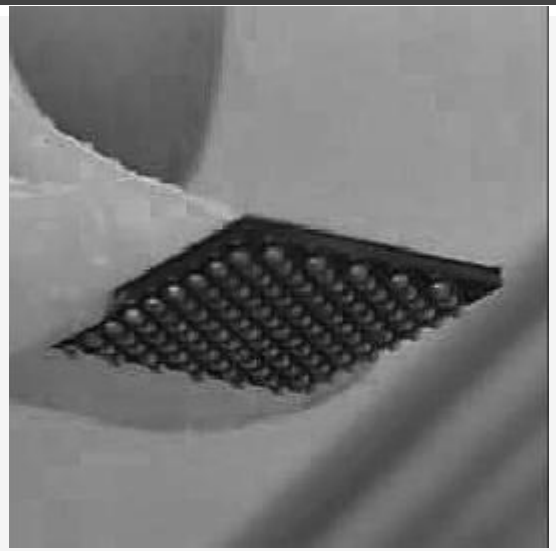
- Back side

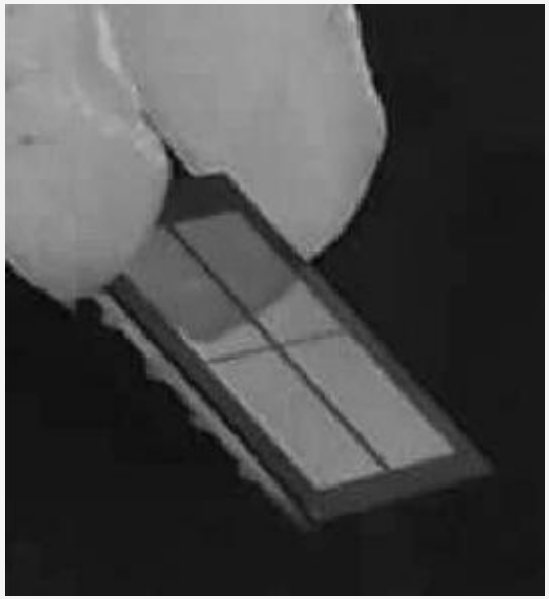




- Screen printed ball cross section
  - Height: 235µm
  - Diameter: 300µm
  - Width at wafer surface: 280µm

FINAL DICING: READY TO MOUNT ON BOARD!





Final demonstrator dies with Bumps and TSV