WP2: System and Technology Specification

Leader: Valeo – Pierre Tisserand
Start: M1
End: M8
WP2: System and Technology Specification

Planned efforts

<table>
<thead>
<tr>
<th>Work package</th>
<th>AMS</th>
<th>VEEM</th>
<th>Crocus</th>
<th>FHG</th>
<th>TUW</th>
<th>UNIFE</th>
<th>AT</th>
<th>MASER</th>
<th>BESI</th>
<th>CEA</th>
<th>UNIPI</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>WP2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>21,0</td>
</tr>
<tr>
<td>Planned</td>
<td>3,0</td>
<td>6,0</td>
<td>1,0</td>
<td>2,0</td>
<td>3,0</td>
<td>1,0</td>
<td>0,5</td>
<td>0,5</td>
<td>1,0</td>
<td>1,0</td>
<td>1,0</td>
<td>2,0</td>
</tr>
<tr>
<td>person.months per participant</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Deliverables

D2.1: M4 ✓  Technical specification for designing the demonstrators 1 and 2 (WP6) and influencing the ATHENIS_3D technology specification (WP3)

D2.2: M4 ✓  Detailed target specification for the process, device and reliability target parameters for the ATHENIS_3D platform

D2.3: M8 ✓  Detailed Specification of Demo car
WP3: 3D TSV & WLP MODULE DEVELOPMENT

Leader: Crocus - Ken McKay

Start: M4
End: M36
## Planned efforts

<table>
<thead>
<tr>
<th>Work package</th>
<th>AMS</th>
<th>VEEM</th>
<th>Crocus</th>
<th>FHG</th>
<th>TUW</th>
<th>UNIFE</th>
<th>AT</th>
<th>MATER</th>
<th>BESI</th>
<th>CEA</th>
<th>UNIPI</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>WP3</td>
<td>20,0</td>
<td>1,0</td>
<td>29,0</td>
<td>28,0</td>
<td>3,0</td>
<td>1,0</td>
<td>0,5</td>
<td>1,0</td>
<td></td>
<td>3,0</td>
<td></td>
<td>86,5</td>
</tr>
</tbody>
</table>

## Deliverables

- **D3.1: M12 ✓**  
  Report on 200V monolithic integrated Capacitors [FHG]
- **D3.2: M22 ✓**  
  Report on fabricated Capacitors including high-k devices [FHG]
- **D3.3: M26 ✓**  
  Report on interposer and IPD integration of uH inductors with TSV technology [FHG]
- **D3.4: M42 ✓**  
  Summary of performances/cost ratio of integrated discretes [VEEM]
- **D3.5: M22 ✓**  
  Report on MRAM technology extended to automotive requirem. [Crocus]
- **D3.6: M18 ✓**  
  Report on scalable reverse polarity HVCMOS technology [AMS]
### WP3: Task Overview

| Task T3.1: Design and development of high-density Si-integrated capacitors [FhG] |
|-------------------------------|---|---|
| Start: M4                    | End: M12 | $\rightarrow$ D3.1, M12 | ✔ |

| Task T3.2: Fabrication and characterisation of high-density Si-integrated capacitors [FhG] |
|-------------------------------|---|---|
| Start: M12                    | End: M21 | $\rightarrow$ D3.2, M22 | ✔ |

| Task T3.3: Development of integrated inductances using TSV technology [FhG] |
|-------------------------------|---|---|
| Start: M12                    | End: M24 | $\rightarrow$ D3.3, M26 | ✔ |

| Task T3.4: Evaluation of device performance/cost-ratio for Si integrated L&C [VEEM] |
|-------------------------------|---|---|
| Start: M15                    | End: M42 | $\rightarrow$ D3.4, M42 | ✔ |

| Task T3.5: extension of MRAM NVM to meet 200C automotive requirements [Crocus] |
|-------------------------------|---|---|
| Start: M4                     | End: M24 | $\rightarrow$ D3.5, M22 | ✔ |

| Task T3.6: implementation of scalable HVCMOS devices [AMS] |
|-------------------------------|---|---|
| Start: M4                     | End: M18 | $\rightarrow$ D3.6, M18 | ✔ |
T3.1 – Design of integrated capacitors

- Deliverable 3.1 was completed in M12

- Goal
  - Thermal mechanical simulation to account for and control wafer bow during fabrication of high density integrated capacitors

- Achievements
  - Extensive multi-scale device simulations
  - Include residual stresses
  - Composite material
Deliverable 3.2 was completed in M22

Summary
- Desired integration density achieved 100nF/mm$^3$
- TSV-based capacitors – via diameter 8µm/10µm – via depth 74µm
- Chip areas: 9mm$^2$ and 2.15mm$^2$

48V Capacitors
- Dielectric: 20nm SiO$_2$ / 73nm Si$_3$N$_4$ – Integration density: 96nF/mm$^3$
- Use voltage: 45V, Breakdown voltage: 95V (0.11MJ/m$^3$)
- Wafer bow: < 220µm

96V Capacitors
- Dielectric: 20nm SiO$_2$ / 184nm Si$_3$N$_4$ – Integration density: 54nF/mm$^3$
- Use voltage: >100V (0.25MJ/m$^3$)
T3.1 & 2 – Electrical properties of fabricated capacitors

- **Device structure**
  - Junction isolated capacitors
  - Hole patterns confined within each chip
  - Hole patterning masks only by resist
  - Metal patterned by lithography (instead of shadow mask)

- **Chip layout**
  - E12 capacitor series
  - 10-100nF
  - Metal patterning by mask aligner
  - Different exposed areas: 1 – 50% (pattern load)
Characterisation Results

- High density achieved
- Good isolation achieved
- Used for 3D stacking in WP5
T3.3 – Development of integrated inductances using TSV technology [FhG]

- Deliverable D3.3 was completed in M26

- Summary
  - Low parasitic resistance essential
  - Modeling and simulation (ANSYS Q3D Extractor)

- Achievements: quality factor > 200

<table>
<thead>
<tr>
<th>Model</th>
<th>w/o TSV</th>
<th>1 TSV</th>
<th>Continuous-TSVs</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV-diameter [µm]</td>
<td>no TSV</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>TSV-depth [µm]</td>
<td>no TSV</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Material</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
</tr>
<tr>
<td>Cross-section dimension [µm2]</td>
<td>10x80</td>
<td>10x80</td>
<td>10x80</td>
</tr>
<tr>
<td>Distance between each ring [µm]</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Number of turns</td>
<td>24</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Volume [mm3]</td>
<td>3.92</td>
<td>1.80</td>
<td></td>
</tr>
<tr>
<td>Inductance [µH]</td>
<td>1.04</td>
<td>1.03</td>
<td></td>
</tr>
<tr>
<td>Inductance density [nH/mm3]</td>
<td>264.25</td>
<td>574.11</td>
<td></td>
</tr>
<tr>
<td>Series resistance [Ohm]</td>
<td>4.23</td>
<td>3.82</td>
<td></td>
</tr>
<tr>
<td>Resonance frequency [MHz]</td>
<td>375</td>
<td>420</td>
<td></td>
</tr>
<tr>
<td>Quality factor</td>
<td>7.61</td>
<td>8.47</td>
<td></td>
</tr>
</tbody>
</table>
Now covered in WP6
D3.5 – High Temperature Automotive MRAM

- Deliverable D3.5 was completed in M22 (2015-08-31)

- Summary
  - High temperature magnetic materials developed
  - Good retention and endurance demonstrated (WP8)
  - W/R performance characterised
  - Process integration flow identified
  - 1K and 32K test chips provided for WP8
Challenges

- Magnetic Materials
  - Engineered high thermal stability
  - Multiple stacks evaluated
- Process integration
  - Contamination compatible flow identified

Achievements

- Device design
  - Thermal response
- Device Characterisation
  - Write/Read parameters determined
  - 2 write modes identified
  - 1K & 32K samples prepared for WP8
Deliverable D3.6 was completed in M18

- **Summary**
  - Voltage scalable extended to 0.18µm HVCMOS.
  - Required new methods to account for different LDMOS HV transistor device structures

- **Achievements**
  - Optimized transistors can now be chosen to select between required breakdown voltage BV and the minimum On-resistance Ron for the H-bridge driver application

- **Decision Matrix**
  - Choose 0.35µm for project
  - Better reliability – lower risk