ATHENIS 3D

# WP2: System and Technology Specification

| | |
|---|---|
| **Leader:** | **Valeo – Pierre Tisserand** |
| Start: | M1 |
| End: | M8 |

# WP2: System and Technology Specification

## Planned efforts

| Work package | | AMS | VEEM | Crocus | FHG | TUW | UNIFE | AT | MASER | BESI | CEA | UNIPI | Total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **WP2** | Planned person.months per participant | **3,0** | 6,0 | **1,0** | 2,0 | 3,0 | 1,0 | 0,5 | 0,5 | 1,0 | 1,0 | **2,0** | **21,0** |

## Deliverables

D2.1: M4 ✓ Technical specification for designing the demonstrators 1 and 2 (WP6) and influencing the ATHENIS_3D technology specification (WP3)

D2.2: M4 ✓ Detailed target specification for the process, device and reliability target parameters for the ATHENIS_3D platform

D2.3: M8 ✓ Detailed Specification of Demo car

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# WP3: 3D TSV & WLP MODULE DEVELOPMENT

| | |
|---|---|
| **Leader:** | **Crocus - Ken McKay** |
| Start: | M4 |
| End: | M36 |

# WP3: IPD, HV, and NVM DEVELOPMENT



## Planned efforts

| Work package | | AMS | VEEM | Crocus | FHG | TUW | UNIFE | AT | MASER | BESI | CEA | UNIPI | Total |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WP3 | Planned person.months per participant | 20,0 | 1,0 | 29,0 | 28,0 | 3,0 | 1,0 | 0,5 | 1,0 | | 3,0 | | 86,5 |

## Deliverables

| | |
|---|---|
| D3.1: M12 ✓ | Report on 200V monolithic integrated Capacitors [FHG] |
| D3.2: M22 ✓ | Report on fabricated Capacitors including high-k devices [FHG] |
| D3.3: M26 ✓ | Report on interposer and IPD integration of uH inductors with TSV technology [FHG] |
| D3.4: M42 ✓ | Summary of performances/cost ratio of integrated discretes [VEEM] |
| D3.5: M22 ✓ | Report on MRAM technology extended to automotive requirem. [Crocus] |
| D3.6: M18 ✓ | Report on scalable reverse polarity HVCMOS technology [AMS] |

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# WP3: Task Overview

**Task T3.1: Design and development of high-density Si-integrated capacitors [FhG]**

Start: M4 End: M12 → **D3.1, M12** ✓

**Task T3.2: Fabrication and characterisation of high-density Si-integrated capacitors [FhG]**

Start: M12 End: M21 → **D3.2, M22** ✓

**Task T3.3: Development of integrated inductances using TSV technology [FhG]**

Start: M12 End: M24 → **D3.3, M26** ✓

**Task T3.4: Evaluation of device performance/cost-ratio for Si integrated L&C [VEEM]**

Start: M15 End: M42 → **D3.4, M42** ✓

**Task T3.5: extension of MRAM NVM to meet 200C automotive requirements [Crocus]**

Start: M4 End: M24 → **D3.5, M22** ✓

**Task T3.6: implementation of scalable HVCMOS devices [AMS]**

Start: M4 End: M18 → **D3.6, M18** ✓

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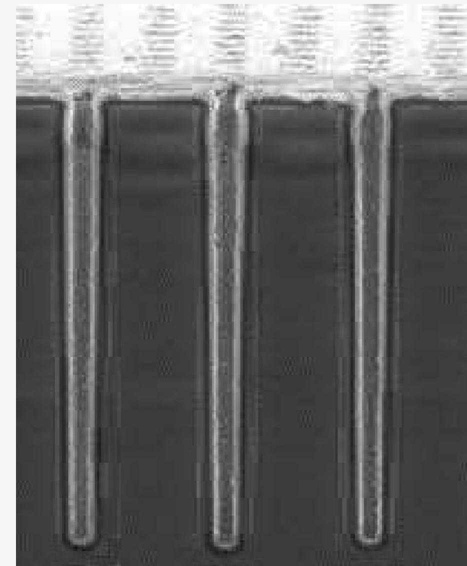
# T3.1 – Design of integrated capacitors

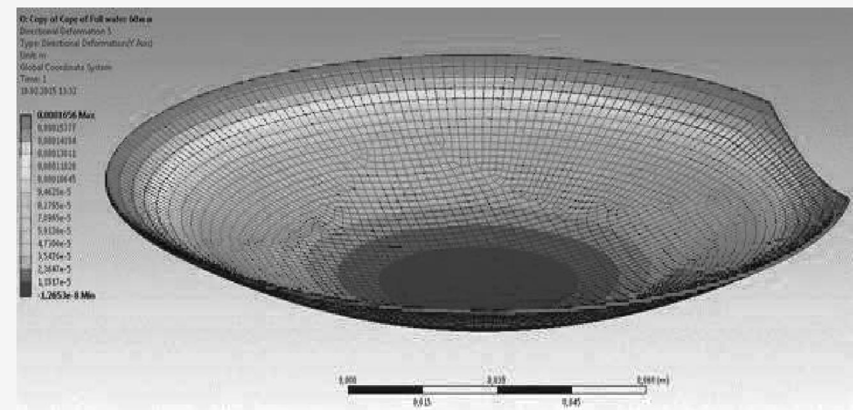


- Deliverable 3.1 was completed in M12

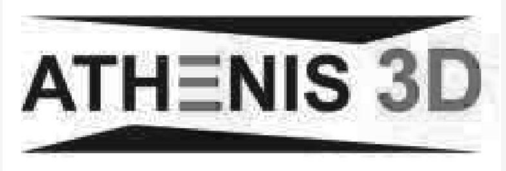


- Goal
  - Thermal mechanical simulation to account for and control wafer bow during fabrication of high density integrated capacitors

- Achievements
  - Extensive multi-scale device simulations
  - Include residual stresses
  - Composite material



# T3.1&2 – Design, fabrication and characterisation of integrated capacitors [FhG]






- Deliverable 3.2 was completed in M22

- Summary
  - Desired integration density achieved **100nF/mm$^3$**
  - TSV-based capacitors – via diameter 8µm/10µm – via depth 74µm
  - Chip areas: 9mm$^2$ and 2.15mm$^2$
- 48V Capacitors
  - Dielectric: 20nm $SiO_2$ / 73nm $Si_3N_4$ – Integration density: 96nF/mm$^3$
  - Use voltage: 45V, Breakdown voltage: 95V (0.11MJ/m$^3$)
  - Wafer bow: < 220µm
- 96V Capacitors
  - Dielectric: 20nm $SiO_2$ / 184nm $Si_3N_4$ – Integration density: 54nF/mm$^3$
  - Use voltage: >100V (0.25MJ/m$^3$)

# T3.1&2 – Electrical properties of fabricated capacitors

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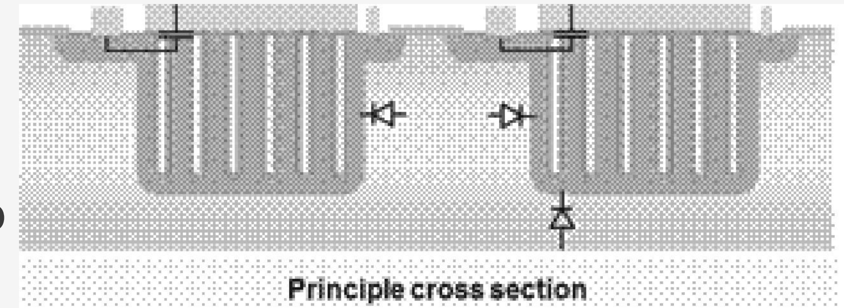
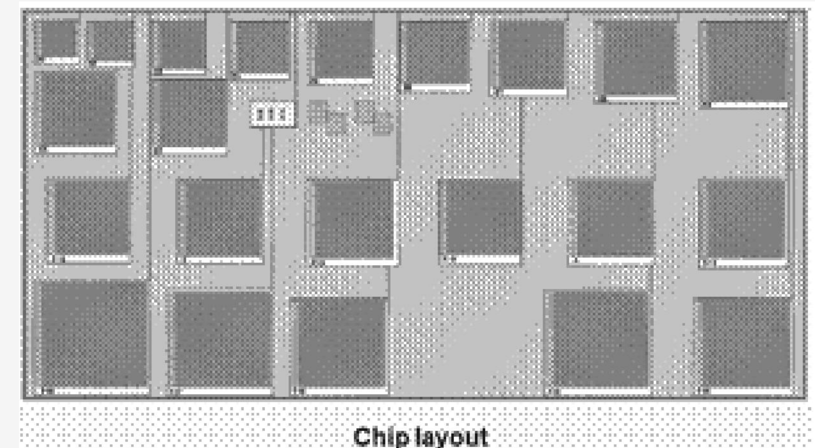
- Device structure
  - Junction isolated capacitors
  - Hole patterns confined within each chip
  - Hole patterning masks only by resist
  - Metal patterned by lithography (instead of shadow mask)

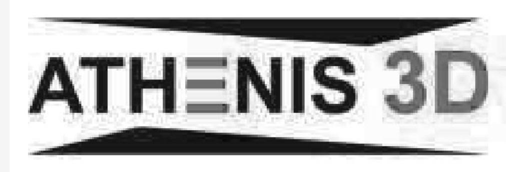



*Schematic cross-section of lateral TSV capacitor*

- Chip layout
  - E12 capacitor series
  - 10-100nF
  - Metal patterning by mask aligner
  - Different exposed areas: 1 – 50% (pattern load)



# T3.2 – Fabrication and characterisation of Integrated Capacitors





- Characterisation Results
  - High density achieved
  - Good isolation achieved
  - Used for 3D stacking in WP5

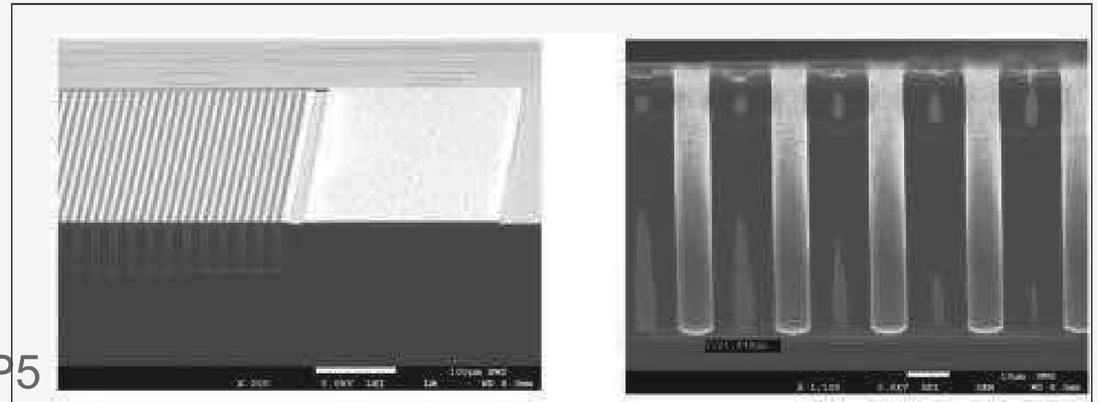


Figure 3.2.5: SEM images of the fabricated silicon trench capacitors

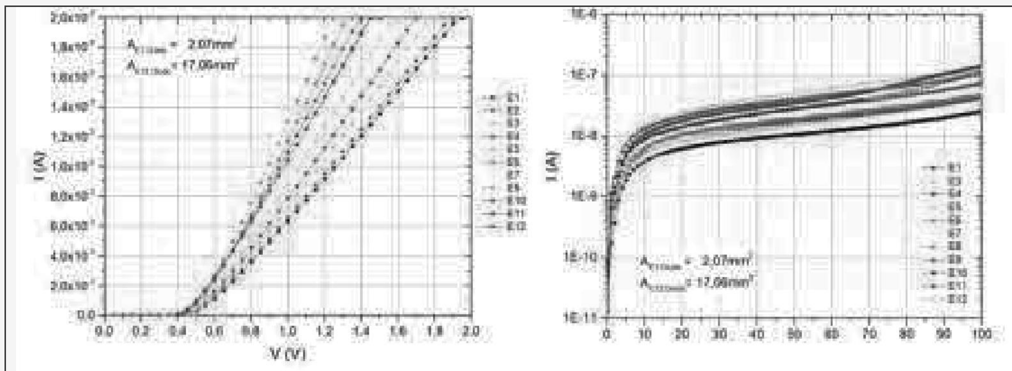


Figure 3.2.4: Forward and reverse properties of integrated body diode in the lateral trench capacitor process

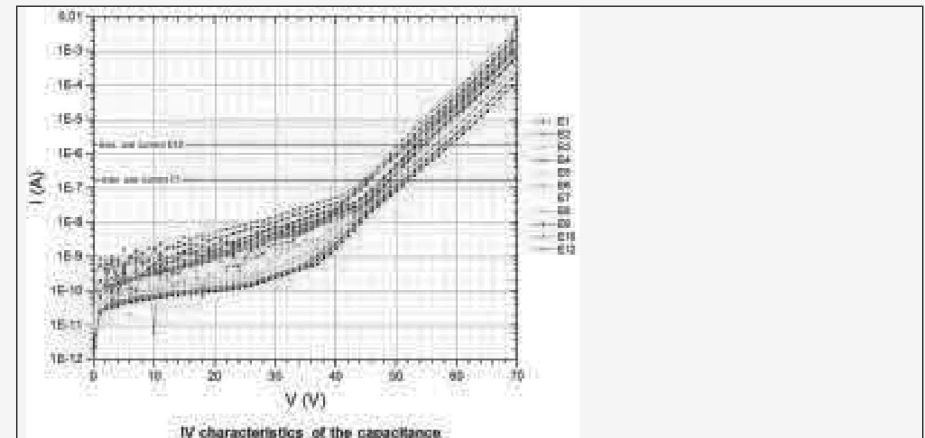
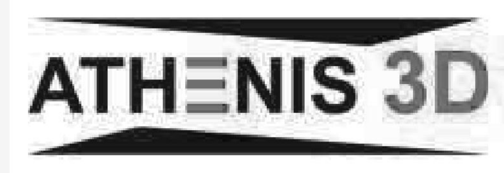


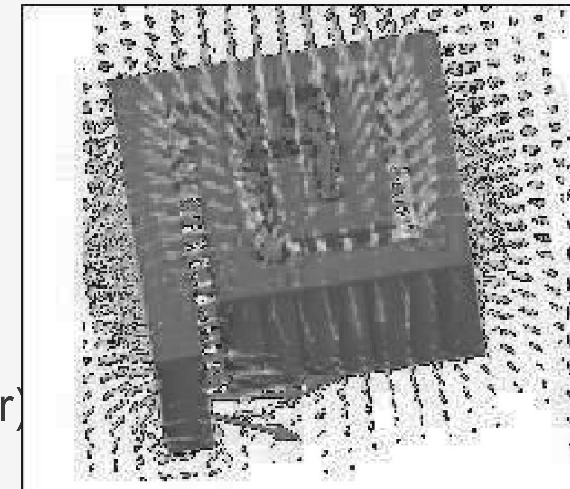

Figure 3.2.2: Leakage current through the lateral integrated trench silicon capacitors

# T3.3 – Development of integrated inductances using TSV technology [FhG]



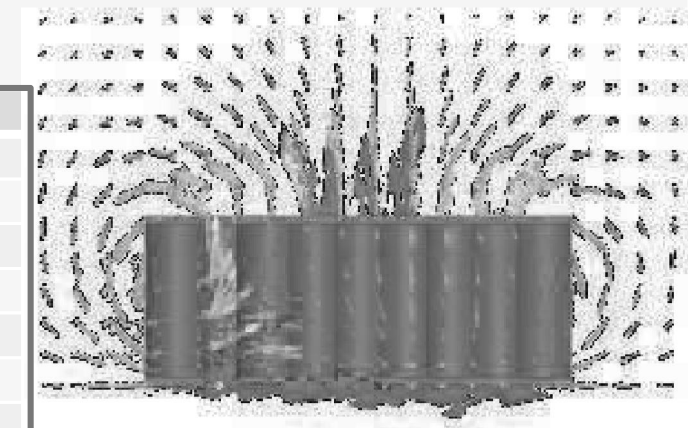



- Deliverable D3.3 was completed in M26



- Summary
  - Low parasitic resistance essential
  - Modeling and simulation (ANSYS Q3D Extractor)

- Achievements : quality factor > 200



| Model | w/o TSV | 1 TSV | Continuous-TSVs |
|---|---|---|---|
| TSV-diameter [µm] | no TSV | 80 | 80 |
| TSV-depth [µm] | no TSV | 200 | 200 |
| Material | Cu | Cu | Cu |
| Cross-section dimension [µm2] | 10x80 | 10x80 | 10x80 |
| Distance between each ring [µm] | 20 | 20 | 20 |
| Number of turns | 24 | 16 | 27 |
| Volume [mm3] | 3.92 | 1.80 | 5.19 |
| Inductance [µH] | 1.04 | 1.03 | 1.10 |
| Inductance density [nH/mm3] | 264.25 | 574.11 | 211.71 |
| Series resistance [Ohm] | 4.23 | 3.82 | 0.16 |
| Resonance frequency [MHz] | 375 | 420 | 333 |
| Quality factor | 7.61 | 8.47 | 221.01 |

# T3.4: Evaluation of device performance/cost-ratio for Si-integrated capacitors and inductors [Leader: VES]

Now covered in WP6

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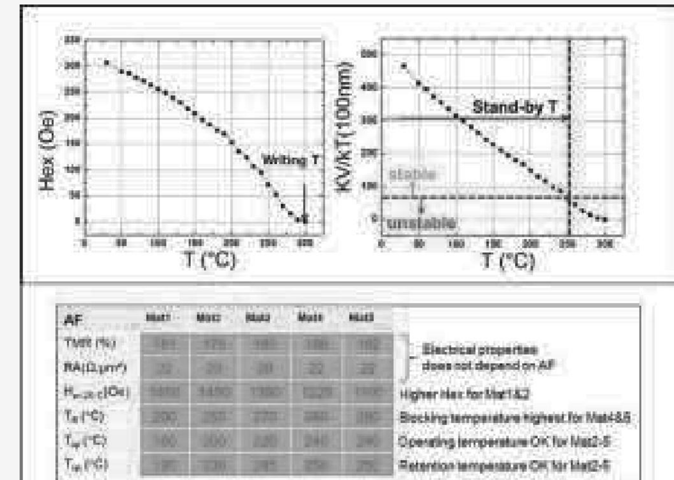
# D3.5 – High Temperature Automotive MRAM

- Deliverable D3.5 was completed in M22 (2015-08-31)

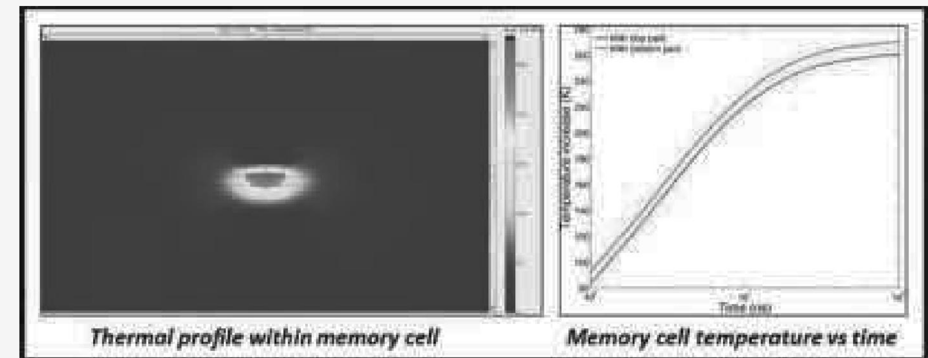
- Summary
  - High temperature magnetic materials developped
  - Good retention and endurance demonstrated (WP8)
  - W/R performance characterised
  - Process integration flow identified
  - 1K and 32K test chips provided for WP8

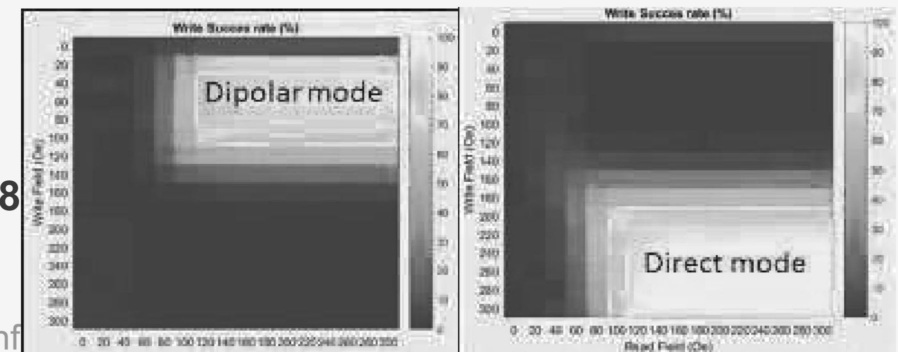
# D3.5 – High Temperature Magnetic NVM

- Challenges
  - Magnetic Materials
    - Engineered high thermal stability
    - Multiple stacks evaluated
  - Process integration
    - Contamination compatible flow identified

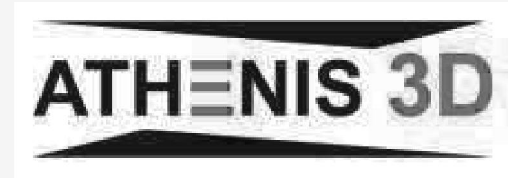



- Achievements
  - Device design
    - Thermal response
  - Device Characterisation
    - Write/Read parameters determined
    - 2 write modes identified
    - **1K & 32K samples prepared for WP8**


Thermal profile within memory cell
Memory cell temperature vs time



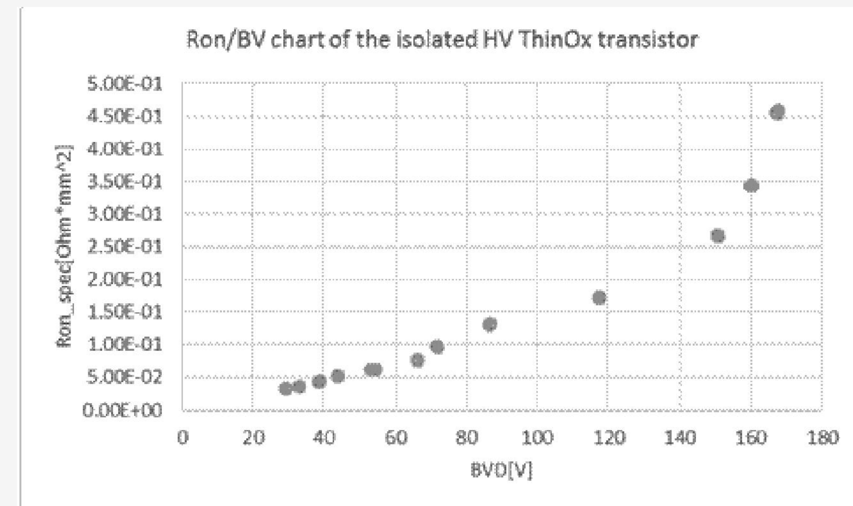
# T3.6 Implementation of scalable HVCMOS devices [Leader: AMS]






Deliverable D3.6 was completed in M18

- Summary
  - Voltage scalable extended to 0.18µm HVCMOS.
  - Required new methods to account for different LDMOS HV transistor device structures




- Achievements
  - optimized transistors can now be chosen to select between required breakdown voltage BV and the minimum On-resistance Ron for the H-bridge driver application

- Decision Matrix
  - Choose 0.35um for project
  - Better reliability – lower risk

| | 0.35µm HVCMOS | 0.18µm HVCMOS |
|---|---|---|
| **Voltage Scalable transistors** | available | available |
| **Reliability based operating conditions** | available | in development |
| **SPICE models** | available | partially |
| **ESD library** | available | in development |
| **3D integration compatible** | proven | in development |
| **Size advantage** | 0 | ~ 10% area saving |