Welcome to the final review meeting !

@ ams AG, Premstätten, Austria

Automotive Tested High Voltage and Embedded Non-Volatile Integrated System on Chip platform employing 3D Integration

Coordinator: **ams AG** **Ewald Wachmann**

Participants

EC / Reviewer	Eric Fribourg-Blanc, Riccardo Groppo, Grigore Danciu
AMS:	Ewald Wachmann, Jörg Siegert, Karin Ronijak
ACT:	Michele Ramponi
BESI:	Zlatko Hajderevic
CEA:	Jean Charbonnier
CROCUS:	Ken Mackay
FHG IIS:	Norbert Schuhmann
FHG IISB:	Peter Pichler, Tobias Erlbacher
MASER:	Kees Revenberg
TU VIENNA:	Markus Jech
UNI Ferrara:	Cristian Zambelli
Uni Pisa:	Sergio Saponara
Valeo:	Dieu-My Ton, Pierre Tisserand (by phone)

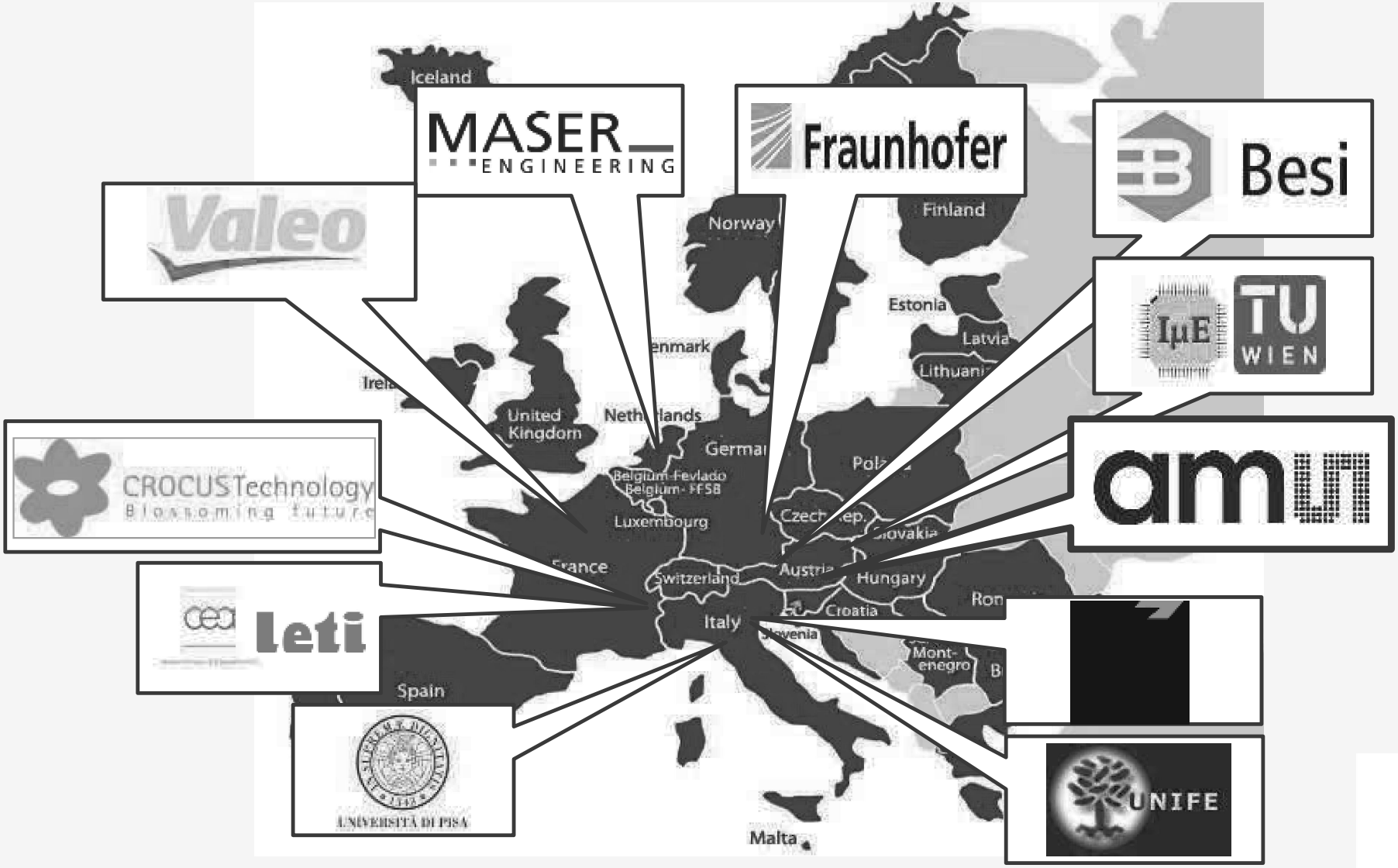
Agenda: morning

09:00 – 09:30	**Meeting of European Commission and reviewers**	
09:30 – 09:45	**Welcome & Introduction (tour de table)**	Ewald Wachmann
09:45 – 10:15	**Project overview by the coordinator** Project objectives and achieved results	Ewald Wachmann
10:15 – 10:30	**Coffee break**	
10:30 – 10:45	**WP3 IPD, HV and NVM Development** (Start M4) Scope of WP and achieved results	Ken McKay
10:25 – 11:20	**WP4 3D/TSV & WLP Development** (Start M4) Scope of WP and achieved results D4.4, D4.5, D4.6	Jean Charbonnier
11:20 – 12:00	**WP5 Testchip Development** (Start M7) Scope of WP and achieved results D5.2, D5.3, D5.4, D5.5,	Sergio Saponara Ewald Wachmann Norbert Schumann
12:00 – 12:40	Lunch break	

Agenda: afternoon

12:40 – 13:10	**WP6 Process and Platform Integration** (Start M9) Scope of WP and achieved results D6.2, D6.4, D3.4, D6.5	Jörg Siegert, Dieu-My Ton
13:10– 13:35	**WP7 System Development and Evaluation** (Start M7) Scope of WP and achieved results D7.1, D7.2, D7.3	Dieu-My Ton, Pierre Tisserand (by phone)
13:35– 14:00	**WP8 Characterization and Reliability** (Start M9) Scope of WP and achieved results D8.3, D8.4, D8.5, D8.6	Cristian Zambelli Markus Jech Kees Revenberg Norbert Schuhmann
14:00 – 14:15	**WP9 Dissemination and Exploitation** (Start M1) Scope of WP and achieved results Presentation of project movie D9.6, D9.7, D9.8	Karin Ronijak
14:15 – 14:40	**Summary / Cost status / pm-list** Conclusions & Questions	Ewald Wachmann
14:40 – 15:15	Deliberation of EC and reviewers	
15:15 – 15:30	brief oral feedback by the EC PO	Project officer
15:30	Meeting close	
	Optional company tour	

Project consortium



SEVENTH FRAMEWORK PROGRAMME

WP Leaders

Workpackage	Title	WP Leader
WP1	PROJECT COORDINATION	Ewald Wachmann, AMS
WP2	SYSTEM AND TECHNOLOGY SPECIFICATION	Pierre Tisserand, Valeo
WP3	IPD, HV and NVM DEVELOPMENT	Ken Mackay, Crocus
WP4	3D/TSV & WLP DEVELOPMENT	Jean Charbonnier, CEA Leti
WP5	TESTCHIP DEVELOPMENT	Sergio Saponara, UNIPI
WP6	PROCESS AND PLATFORM INTEGRATION	Jörg Siegert, AMS
WP7	SYSTEM DEVELOPMENT AND EVALUATION	Pierre Tisserand, Valeo
WP8	CHARACTERIZATION AND RELIABILITY	Cristian Zambelli, UNIFE
WP9	DISSEMINATION AND EXPLOITATION	Karin Ronijak, AMS

Amendment & Changes

ATHENIS_3D has been started in Oct 2013

Two amendments were required for content and for extended duration

- **DoW Amendment 1**
    - H-bridge demonstrator + control concept
    - NanoCMOS on interposer with WLOM
    - MRAM process integration
- **DoW Amendment 2**
    - duration extended for 6 months to correct HD interposer scaling factor

DoW amendment 1

Changes:

H-bridge demonstrator

- Definition of the 3D integrated H-bridge demonstrator with controller turned out to be more challenging and cost and resource-intensive than anticipated. Therefore it was agreed to limit the scope for the H-bridge driver design only to a conceptual study enabling future industrialization for instance as part of an innovation pilot project.

- H-bridge demonstrator control in demo car will be realized by a discrete concept from Valeo

- Development of H-bridge MOSFET driver concept and schematic subcontracted to **UPMC** Université Pierre et Marie CURIE. This included slew rate control di/dt control for high-side MOS switching, temperature and current measurements of the power MOS and reverse polarity breakdown protection.

DoW amendment 1

Changes:

NanoCMOS on interposer with WLOM

- The development of 3D integration concept of high density interposers as required for advanced NanoCMOS chips has shown the necessity to introduce wafer level over molding WLOM to enable the process sequences for frontside die stacking and backside interconnect processing.

- Therefore a task for WLOM development has been included in WP4

MRAM

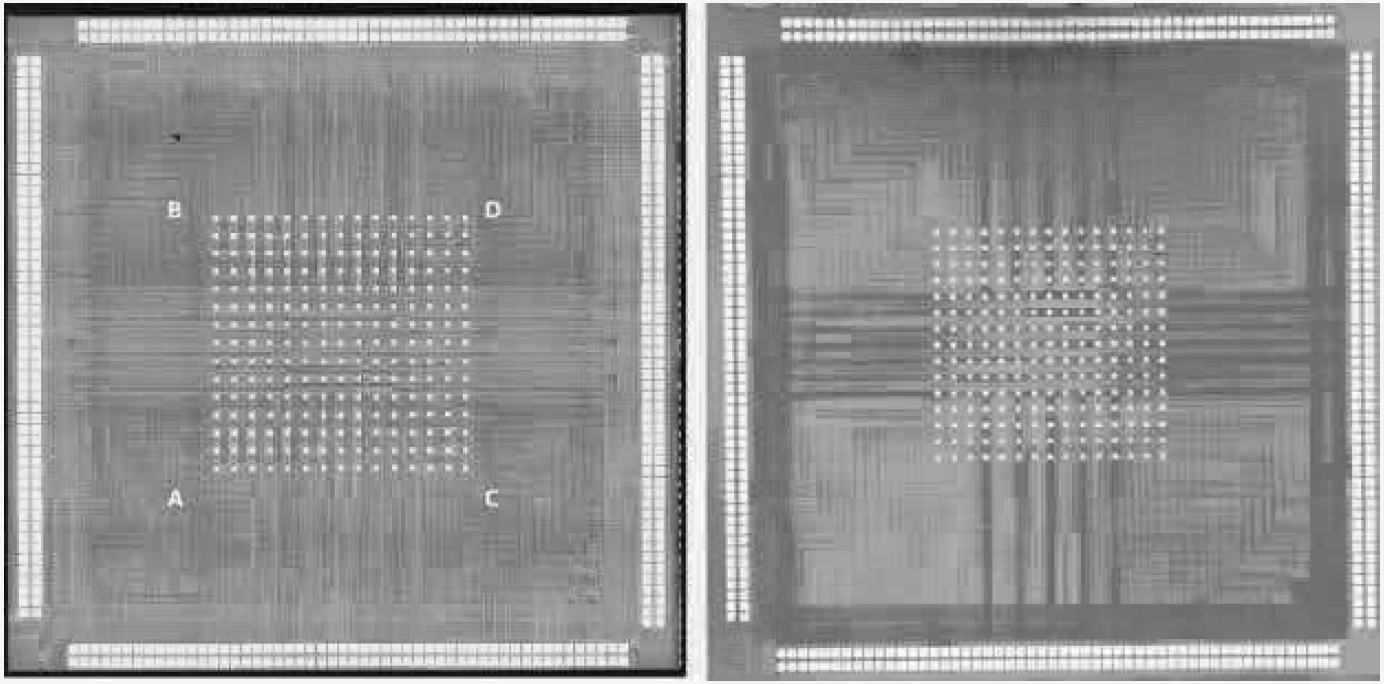
- The post processing of wafers with MRAM layers in the AMS CMOS fab is limited due to contamination concerns. A post processing flow to finalize the interconnects on top of the MRAM layers has been worked out at partner CEA LETI

- Although the final integration process flow was worked out the targeted design of MRAM embedded on 0.18µm HV-CMOS would have needed more resources than available in this task for Crocus. Development of high temperature MRAM was therefore done on samples in the existing flow and provided to the project partners for evaluation

DoW amendment 2 extended duration + 6months

NanoCMOS on HD interposer

- During the first stacking experiments at project partner BESI we learnt that the grid dimension of the landing pads for the SOC28 did not fit with the finally delivered dies prepared for flip chip stacking from GlobalFoundries.
- It could be verified and was confirmed by the subcontracting foundry partner, that for the design a 32nm design kit is provided, where the foundry performs afterwards a 10% shrink for mask preparation.
- Additional iteration for HD interposer manufacturing and UBM processing was needed



Development goals: new technology modules

- **Scalable HV transistors** with reverse polarity protection with reduced Ron resistances and 3D integration capable
- New high temperature capable **eNVM MRAM** for extended automotive temperatures
- **48V IPD** trench based high density Capacitors and Inductors
- **3D WLP modules** (Cu-TSV/BRDL, D2W and WLOM) developed for extended automotive temperatures
- Advanced **D2W** stacking on **HD interposer**

Development goals: new methods and equipment

- Improved MOSFET device reliability models
- Multiphysics simulation models for process support of 3D based integrations
- New equipment enabling high temperature **reliability investigations**
- Improved **NVM test capabilities** enabling detailed eNVM MRAM testing including high temperature investigations
- Advanced concept for **H-bridge driver control** developed with slew rate control di/dt for high-side MOS switching, temperature and current measurements of the power MOS

Demonstrators for automotive 3D integration

- A **28nm NanoCMOS** based MCU designed and manufactured in Europe verified for extended automotive temperatures and demonstrating improved form factor with high density 3D interposer stacking

- A novel **inductorless 48V DCDC** converter combined with new **trench based high density capacitors**

- 3D integrated HV transistors for **48V H-bridge** on DBC interposer demonstrating reduced Ron resistances enabled by 3D integration concept

- **Proof-of-concept demonstrator** with an electrical belt system generator-alternator for 48V micro/mild hybrid applications