WP9 planned effort and Deliverables

Planned Efforts

Work package		AMS	VEEM	Crocus	FHG	TUW	UNIFE	AT	MASER	BESI	CEA	UNIPI	Total
WP9	Planned person.months per participant	8,0	1,0	1,0	1,0	2,0	1,0	1,0	1,0	1,0	1,0	1,0	19,0

Deliverables

D9.1: M1 ✓ Finalize the Consortium agreement [AMS]
D9.2: M3 ✓ Provide public project web site [AMS]
D9.3: M13 ✓ First annual report on publication, dissemination and exploitation activities [AMS]
D9.4: M18 ✓ Draft exploitation plan to ensure proper exploitation and high market impact (covers system cost, exploitation plans, IP, market trends, standardization) [AMS]
D9.5: M25 ✓ Second annual report on publication, dissemination and exploitation activities [AMS]
D9.6: M42 ✓ Detailed exploitation plan to ensure proper exploitation and high market impact (covers system cost, exploitation plans, IP, market trends, standardization) [AMS]
D9.7: M42 ✓ Final annual report on publication and dissemination
D9.8: M42 ✓ Movie presenting the results of ATHENIS_3D [AMS]

No Milestone in this Workpackage.

WP9: EXPLOITATION

Last reporting periode:

Regular Update of www.athenis3d.eu

Work out a detailed exploitation plan to ensure proper exploitation and high market impact covers system cost

Prepare the final annual report on publication, dissemination and exploitation activities, including summary

Create movie which is presenting the results of ATHENIS_3D

Exploitation highlights

2 Patents filed:

1.) French Patent Application Filing No 1461094, Date 18/11/2014: “Système d’alimentation électrique d’un véhicule automobile et module électronique de commande correspondant”; VALEO, Uni Pisa

2.) Patent EU MFR1045, ID 3294, Date September 2015: “Convertisseur DC-DC intégrable sur silicium avec isolation galvanique capacitive”; VALEO, Uni Pisa (Tisserand, P., Chassard, P.,Saponara, S., Ferrari, L.)

Exploitation highlights

Products & Services for following market fields:

Market fields	Partner involved
Licensing of highly integrated capacitor technology	IISB. AMS
Design support for integrated passives in silicon technology	FhG IISB, AMS
Contract research in the area of thermomechanical simulation of yield and reliability issues in 3D integration	FhG IISB
Contract research in the area of integration of capacitors using Standard CMOS technology	FhG IISB
New efficiency alternator for traditional cars, micro hybrid cars, mild hybrid cars and hybrid cars	Valeo, AMS
Design IP blocks in 28nm technology characterized for applications at temperatures <125°C	FhG IIS
Provision of scalable 180nm HVCMOS platform for foundry access	AMS
3D TSV integration modules for high temperature / automotive applications	AMS / CEA LETI
Manufacturing and licensing of high temperature capable MRAM	Crocus / AMS
Development and Sales of flexible NVM testing equipment	Active Technologies
Reliability Investigation Services extended to temperatures > 200°C	MASER

Dissemination highlights

44 technical publications done

13 poster presentations to large audiences

Up-to-date public website www.athenis3d.eu

Movie – presenting the final results of ATHENIS_3D project:

WP1 Project management

Planned Efforts

Work package		AMS	VEEM	Crocus	FHG	TUW	UNIFE	AT	MASER	BESI	CEA	UNIPI	Total
WP1	Planned person.months per participant	14,0	1,0	1,0	1,0	1,0	0,5	0,5	1,0	0,5	1,0	3,0	24,5

Deliverables

D1.1: M9 ✓ First periodic report [AMS]
D1.2: M18 ✓ Second periodic report and cost statement [AMS]
D1.3: M36 (draft ✓) Final periodic report and cost statement [AMS]

No Milestone in this Workpackage.

D6.5	Specification and commitment done for type of Demo Car	6	Valeo	27	17.06.2016	done
D8.1	Report on testing infrastructure for MRAM NVM characterization	8	AT	18	30.04.2015	done
D9.4	Draft exploitation plan to ensure proper exploitation and high market impact (covers system cost, exploitation plans, IP, market trends, standardization)	9	AMS	18	22.05.2015	done
D3.3	Report on the interposer and IPD integration options of µH inductors using TSV technology	3	FHG	25	03.12.2015	done
D3.4	Summary of performance/cost ratio of integrated discretes	3	Valeo	36	16.06.2017	Shifted to M42 with D6.4
D5.1	Report on Testchip design	5	AMS	27	24.03.2016	done
D8.2	Report on reliability assessment of MRAM NVM modules	8	UNIFE	28	29.02.2016	done
D9.5	Second annual report on publication, dissemination and exploitation activities	9	AMS	25	22.12.2015	done
D4.4	Report on “Process module updates for final 3D/TSV/WLP technology concept”	4	CEA	29	26.04.2016	done
D5.2	Design, fabrication and characterization of circuit blocks using IPDs	5	AMS	36	31.05.2017	Shifted to M42 incl. stacked IPD eval.
D5.3	ESD and EMC chip characterization	5	AMS	37	31.05.2017	Shifted to M42 for SoC28 eval
D5.4	testchip characterization at high temperatures	5	MASER	40	02.06.2017	done
D5.5	Design, fabrication and characterization of controller circuit on 28nm and 14nm node	5	FHG	40	08.06.2017	done
D6.2	Report on “Manufacturing technology flow for WLP”	6	BESI	29	24.04.2016	done
D6.3	Report on “HVCMOS interposer manufacturing technology flow”	6	AMS	27	25.03.2016	Done
D7.1	Demonstrator 1 and 2 prototypes validated at system level	7	Valeo	30		done
D8.3	Benchmarking report on MRAM (ATHENIS_3D) vs. SimpleEE (ATHENIS) modules	8	UNIFE	30	01.04.2016	done

WP1: List of upcoming deliverables

D4.5	Report on TSV and WLP process simulation methodology	4	FHG	32	30.06.2016	done
D8.4	Report on reliability of system-level 3D integration approach	8	TUW	40	30.04.2017	done
D8.5	Report on physical reliability modelling of integrated circuit elements	8	TUW	32	28.06.2016	done
D8.6	Report on reliability assessment of demonstrators at high temperatures	8	MASER	40	31.05.2017	done
D4.6	Report on Wafer Level Over Molding	4	CEA	40	24.03.2017	done
D1.3	Final project report and cost statement	1	AMS	42	21.06.2017	Draft
D6.4	Report on “Evaluation of costs and manufacturability of the ATHENIS_3D technology platform”	6	AMS	40	23.06.2017	done
D7.2	Demonstrator 1 and 2 implemented in a demo car	7	Valeo	36	21.10.2016	done
D7.3	Delivery of the demonstrator evaluation report	7	Valeo	36	09.11.2016	done
D9.6	Detailed exploitation plan to ensure proper exploitation and high market impact (covers system cost, exploitation plans, IP, market trends, standardization)	9	AMS	42	20.06.2017	done
D9.7	Final annual report on publication and dissemination	9	AMS	42	19.06.2017	done
D9.8	Movie presenting the results of ATHENIS_3D	9	AMS	42		available

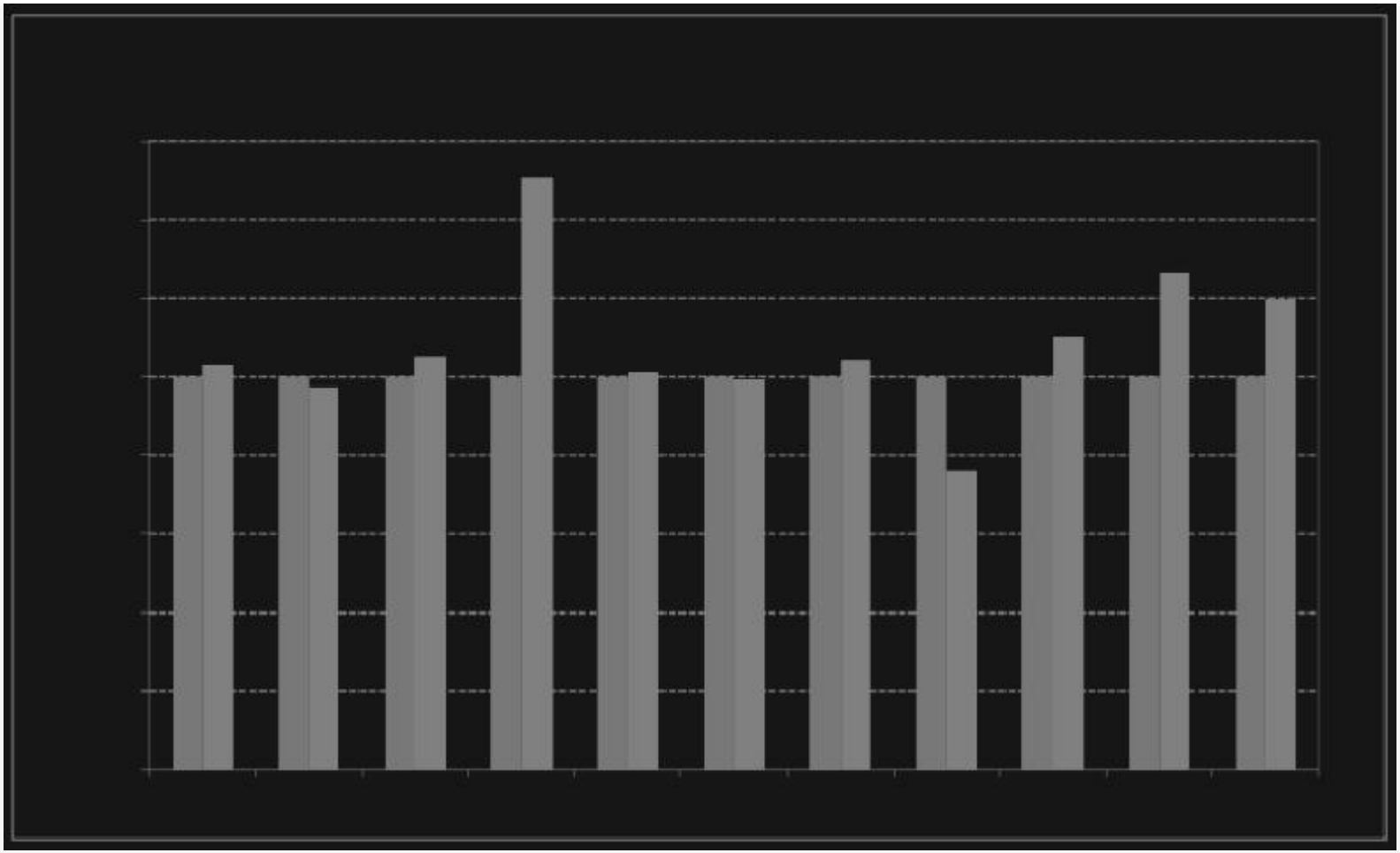
WP1: List of milestones

TABLE 2. MILESTONES							
Mile stone no.	**Milestone name**	**Work package no**	**Lead bene-ficiary**	**Delivery date from Annex I dd/mm/yyyy**	**Achieved Yes/No**	**Actual / Forecast achievement date dd/mm/yyyy**	**Comments**
MS1	System and technology specifications completed	2	**2**	**28/02/2014**	**Yes**	**26/08/2014**	**Additional iterations for demonstrator technology definition were required**
MS2	Detailed specification of Demo Car	2	**2**	**30/06/2014**	**Yes**	**10/07/2014**	
MS3	Development of process modules for platform integration completed	4	**10**	**31/03/2015**	**Yes**	**30/04/2015** **MRAM:** **21/08/2015**	**Selection of required 3D modules described in D443 and D661; MRAM process platform specific fixed by June D335**
MS4	Specification and commitment done for type of Demo Car	6	**2**	**31/01/2016**	**Yes**	**06/01/2016** **Car spec update: 30/06/2016**	**Specifications for car demonstrator D223 updated D665 for car selection update Jun 2016**
MS5	Design of testchips (demonstrator 1 & 2) completed	5	**1**	**31/01/2016**	**Yes**	**31/12/2015**	**HV-bridge transistors, DCDC and SoC28: finished Dec 2015**
MS6	ATHENIS_3D demonstrators implemented and validated in the demo car	7	**2**	**31/10/2016**	**Yes**	**06/10/2016**	**Demonstrator 1 on car validated**

WP1: pm per partner

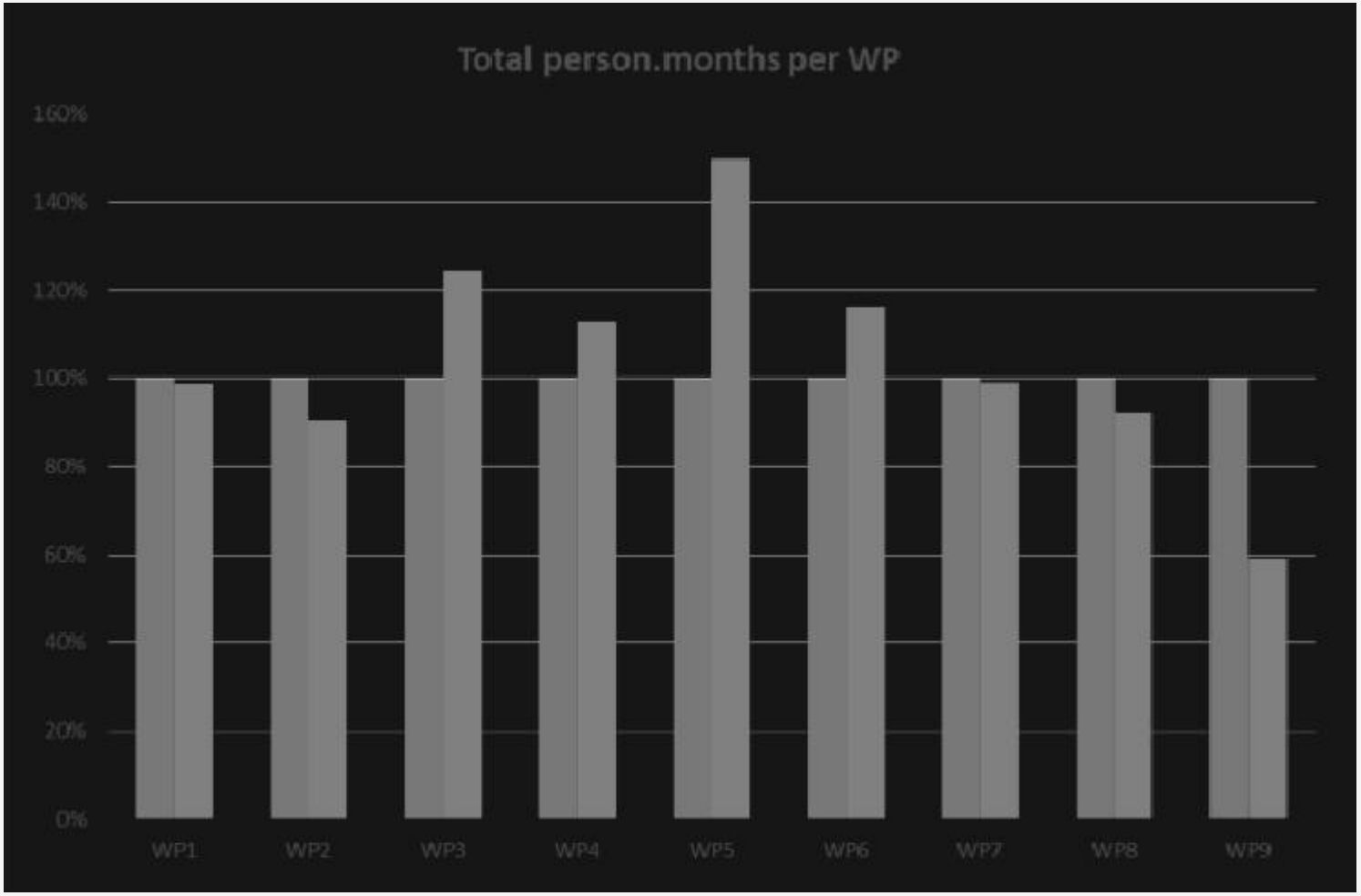
Work package	WP1		WP2		WP3		WP4		WP5		WP6		WP7		WP8		WP9		TOTAL per Beneficiary	
	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total	Actual WP total	Planned WP total
	24,2	24,5	19,0	21,0	107,5	86,5	162,3	143,6	161,8	108,0	65,1	56,0	42,6	43,0	97,6	106,0	11,2	19,0	691,3	607,6
AMS	13,6	**14,0**	2,8	3,0	18,2	20,0	21,0	20,0	17,2	16,5	31,7	**22,0**	2,6	3,0	2,2	3,0	3,2	**8,0**	**112,5**	109,5
VEEM	0,0	1,0	6,0	**6,0**	1,0	1,0	0,0	0,0	12,5	12,5	13,0	13,0	40,0	**40,0**	0,0	0,0	0,0	1,0	**72,5**	74,5
Crocus	1,5	**1,0**	1,2	1,0	28,7	**29,0**	0,0	0,0	0,0	0,0	2,8	2,0	0,0	0,0	3,0	2,0	0,8	1,0	**37,9**	36,0
FHG	1,7	1,0	0,0	2,0	54,1	28,0	16,9	28,0	83,4	43,0	3,0	3,0	0,0	0,0	0,0	0,0	1,0	1,0	**160,0**	106,0
TUW	1,0	1,0	3,0	3,0	3,0	3,0	20,0	20,0	0,0	0,0	3,5	3,0	0,0	0,0	40,3	40,0	2,0	2,0	**72,8**	72,0
UNIFE	0,5	0,5	1,0	1,0	1,0	1,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	21,0	**21,0**	0,9	1,0	**24,4**	24,5
AT	0,6	0,5	1,0	0,5	1,0	0,5	0,0	0,0	0,0	0,0	0,0	0,0	0,0	0,0	19,9	20,0	1,0	1,0	**23,4**	22,5
MASER	1,0	1,0	0,2	0,5	0,6	1,0	0,5	1,0	2,1	0,0	0,0	0,0	0,0	0,0	10,8	15,5	0,0	1,0	**15,2**	20,0
BESI	0,8	0,5	1,3	1,0	0,0	0,0	20,5	18,0	0,0	0,0	10,1	10,0	0,0	0,0	0,0	0,0	0,9	1,0	**33,6**	30,5
CEA	0,5	1,0	0,5	1,0	0,0	3,0	83,4	**56,6**	1,0	3,0	1,0	3,0	0,0	0,0	0,0	0,0	0,5	1,0	**86,9**	68,6
UNIPI	3,0	3,0	2,0	2,0	0,0	0,0	0,0	0,0	45,6	**33,0**	0,0	0,0	0,0	0,0	0,5	4,5	1,0	1,0	**52,1**	43,5

WP1: pm per partner



FhG: The SoC28 design more work intensive as intentionally planned,
SoC28 as vehicle for high temperature more characterization and testing work was required
MASER: The NRE + consumable costs are higher than initially anticipated, personnel effort lower
UNIPI: Additional testing work related to 3 versions of DCDC v1, v2 and 3D version
CEA: additional work related reliability test campaign and WLP studies in terms of overmolding & balling on thin silicon interposer.

WP1: pm per WP


Total person.months per WP
160%
140%
120%
100%
80%
60%
40%
20%
0%
WP1
WP2
WP3
WP4
WP5
WP6
WP7
WP8
WP9

Achievements: new technology modules

- **Scalable HV transistors** with reverse polarity protection demonstrating **>5x** reduced Ron resistances due to new 3D integration concept
- New high temperature capable **MRAM** developed and verified for extended automotive temperatures **>200ºC**
- **48V IPD** trench based high density Capacitors with **100nF/mm³** demonstrated
- **3D WLP modules** (Cu-TSV/BRDL, D2W and **WLOM)** developed for extended automotive temperatures
  ⇨ **a new cornerstone for further automotive or power applications**
- Advanced **D2W** stacking on **HD interposer** (**20µm bump/40µm pitch**) successfully demonstrating progress beyond state-of-the-art

Achievements: new methods and equipment

- Development of worldwide renowned MOSFET **device reliability models** (acknowledged by >24 publications during the last 3 years within ATHENIS_3D)
- Multiphysics simulation models further improved by enhanced material data base enabling process support and new 3D integration concept investigations
- New equipment enabling **reliability investigations** up to **250ºC**
- Improved **NVM test capabilities** enabling detailed eNVM MRAM testing including high temperature characterization
- Advanced concept for **H-bridge driver control schematic** available with slew rate control di/dt for high-side MOS switching, temperature and current measurements of the power MOS

Demonstrators for automotive 3D integration

- A **28nm NanoCMOS** based MCU designed and manufactured in Europe verified for extended automotive temperatures **>175ºC** and demonstrating improved form factor with high density 3D interposer stacking

- A novel **inductorless 48V DCDC** converter combined with new **trench based high density capacitors** successfully verified

- 3D integrated HV transistors for **48V H-bridge** on DBC interposer demonstrating reduced Ron resistance enabled by 3D integration concept

- **Proof-of-concept demonstrator** with an electrical belt system generator-alternator for 48V micro/mild hybrid applications **successfully validated** demonstrating a 5x PCB factor reduction

THANK YOU