ATHENIS 3D

WP8: CHARACTERIZATION AND RELIABILITY

Leader:	**UniFE – Cristian Zambelli**
Start:	M9
End:	M42

WP8 planned effort and Deliverables

Planned Efforts

Work package		AMS	VEEM	Crocus	FHG	TUW	UNIFE	AT	MASER	BESI	CEA	UNIPI	Total
WP8	Planned person.months per participant	3,0		2,0		40,0	21,0	20,0	15,5		0,0	4,5	106,0

Deliverables

D8.1: M18 ✓ Report on Testing infrastructure for MRAM NVM characterization [AT]
D8.2: M28 ✓ Report on Reliability assessment of MRAM NVM modules [UNIFE]
D8.3: M30 ✓ Benchmarking Report on MRAM vs. SimpleEE modules [UNIFE]
D8.4: M40 ✓ Report on Reliability of system-level 3D integration approach [MASER]
D8.5: M32 ✓ Report on physical reliability modelling of integrated circuit elements [TUW]
D8.6: M40 ✓ Report on reliability assessment of MRAM NVM demonstrators at high temperatures [MASER]

Milestone

No milestones

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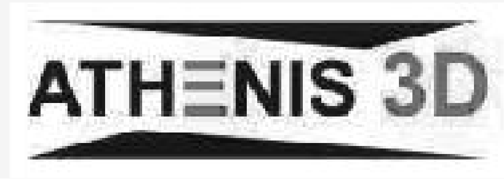
Milestone

No milestones

WP8: T8.1 Hardware and software development for testing NVM modules



Start: M9

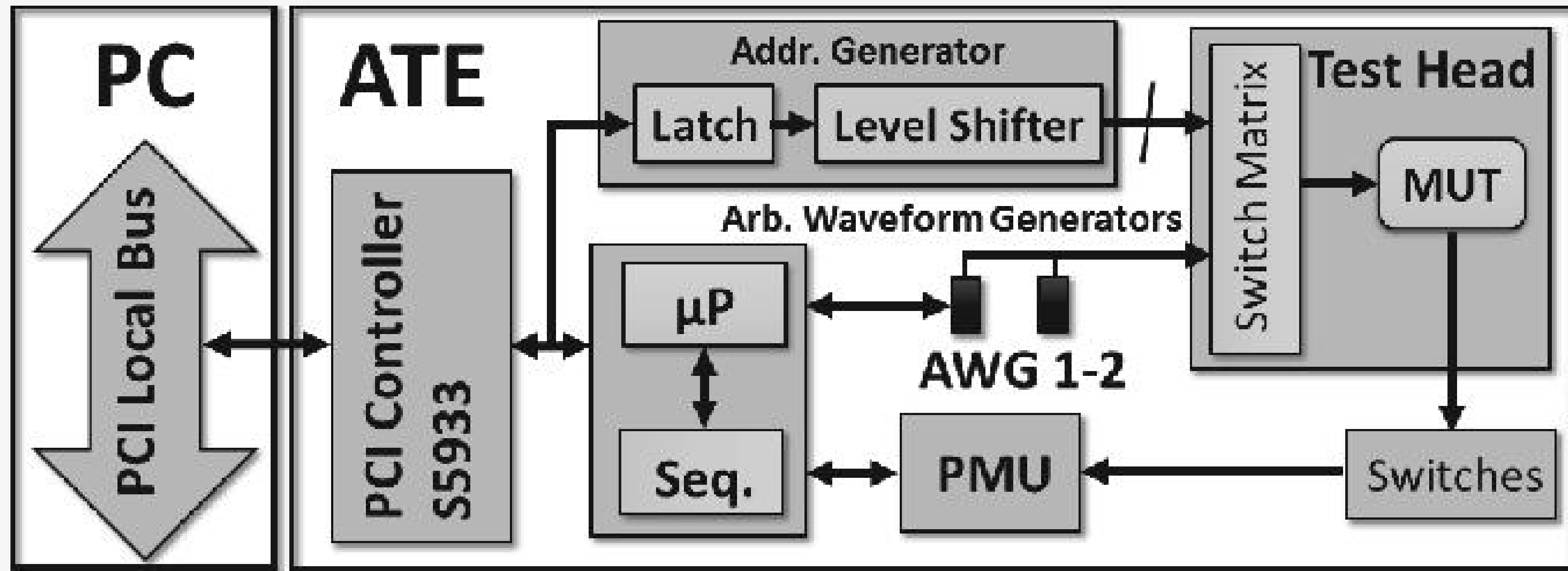
End: M18

RIFLE test system

Objectives:

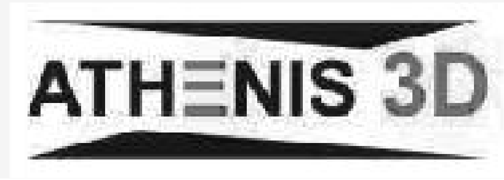
- Development of new architectural and circuit solutions for the RIFLE test equipment suitable for MRAM characterization and reliability tests
- Release of a software driver for the RIFLE system able to communicate with the MRAM module.

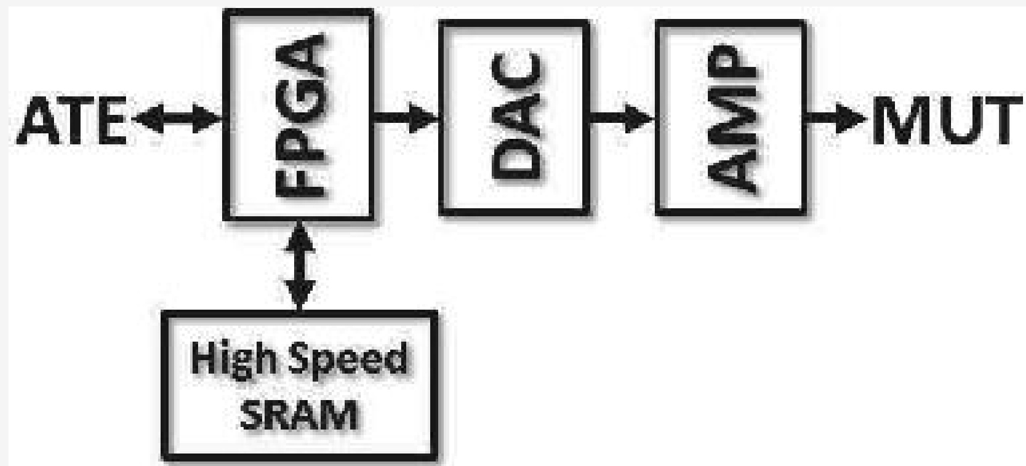
WP8: T8.1 RIFLE ATE architecture



The Automated Test Equipment (ATE) architecture is composed by: PCI controller, RISC µP and Sequencer, two Arbitrary Waveform Generators (AWG) and PMU.

WP8: T8.1 RIFLE ATE Arbitrary Waveform Generators



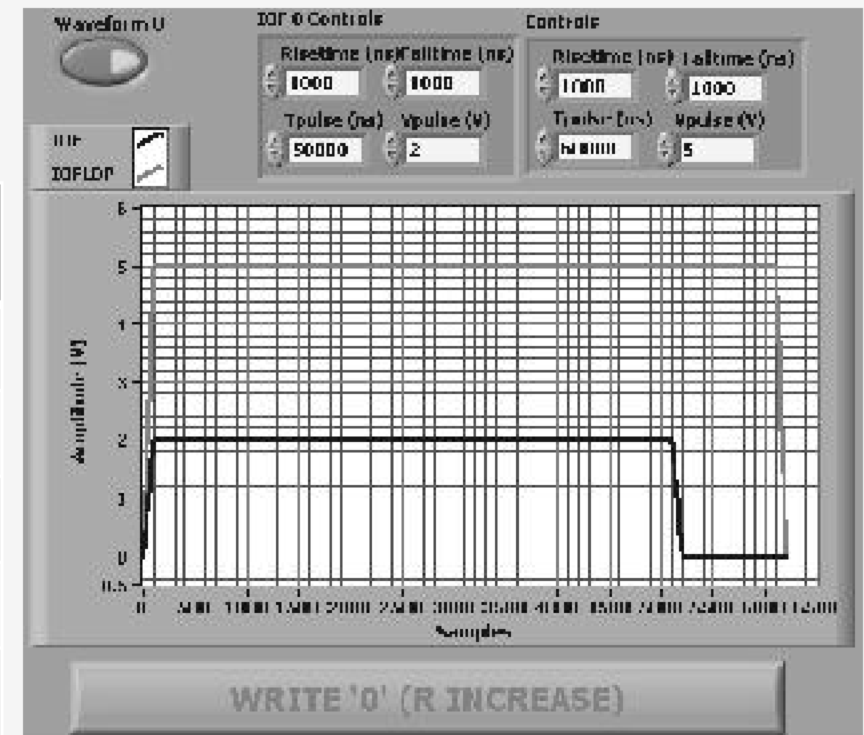


The AWG unit has two independent fully arbitrary waveform generators, operating at up to 100 Mhz (10 ns time resolution), capable of controlling rise and fall time down to 9 ns and voltage resolution down to 1mV.

WP8: T8.1 RIFLE ATE Read and Write Operations

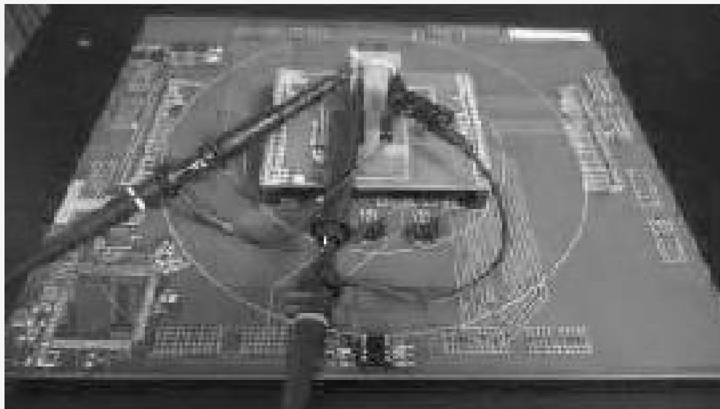
Write and read signals have been used with rise/fall time of 1μs according with device under test specifications.

Operation	Signal	Voltage [V]	Trise [μs]	Thold [μs]	Tfall [μs]
Read	IOF	0.3 V	1 μs	20 μs	1 μs
Write '1'	IOF	2 V	1 μs	50 μs	1 μs
	IOFLDM	5 V	1 μs	60 μs	1 μs
Write '0'	IOF	2 V	1 μs	50 μs	1 μs
	IOFLDP	5 V	1 μs	60 μs	1 μs

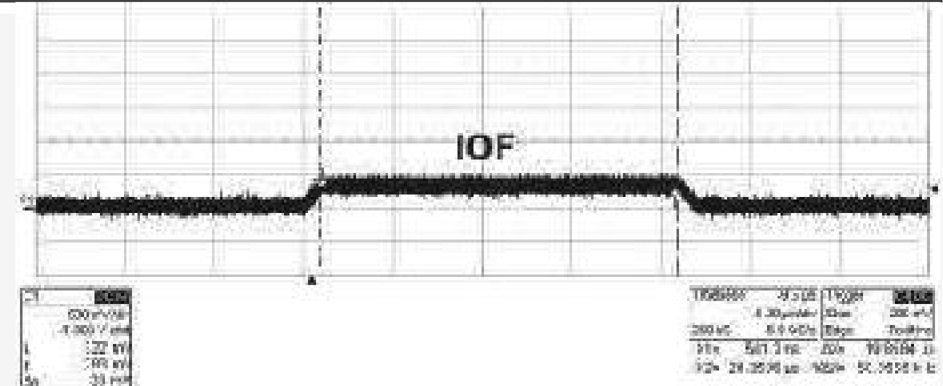


WP8: T8.1 RIFLE ATE Read and Write Operations

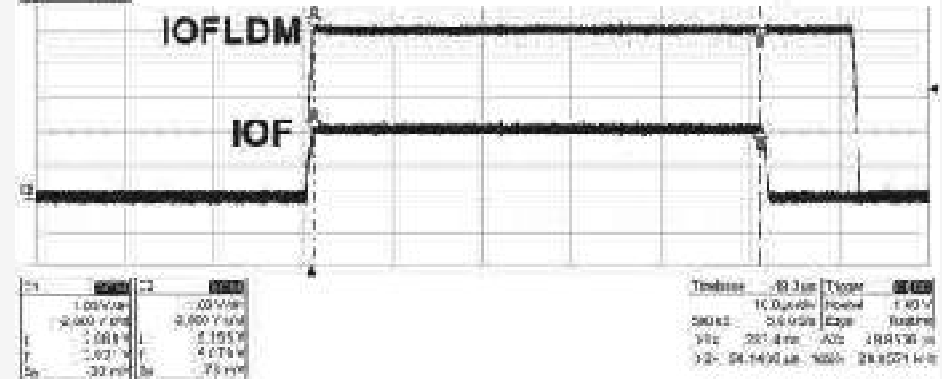
Signals generated during read, write ’0’ and write ’1’ operations through AWGs have been measured with oscilloscope.



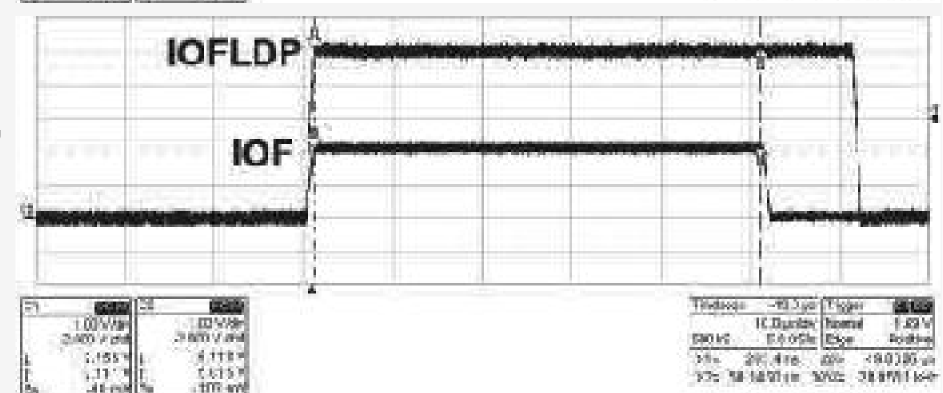
Read



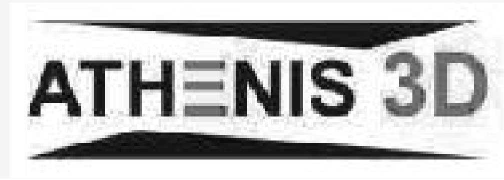
Write ‘1’



Write ‘0’



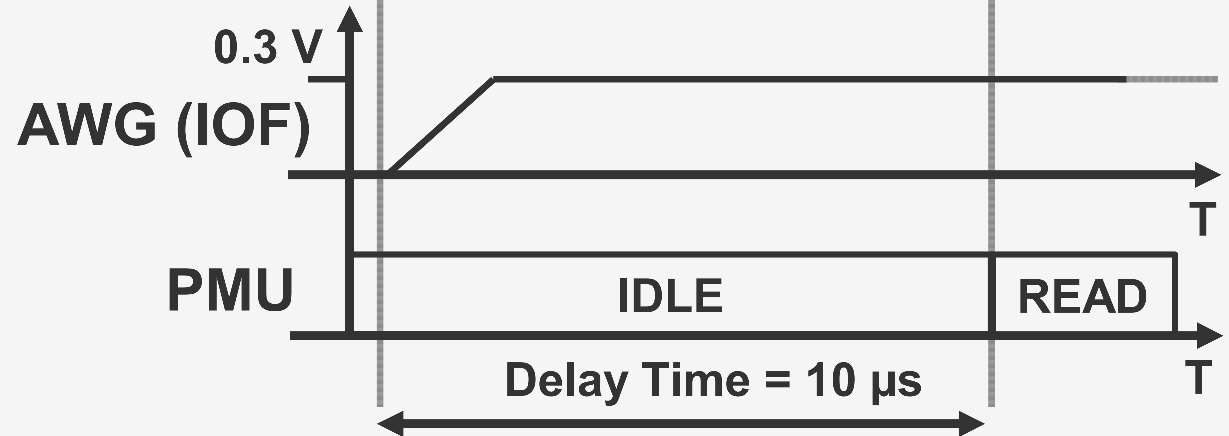
WP8: T8.1 RIFLE ATE RISC Processor and Sequencer



RISC processor allows sharing tasks with the PC.

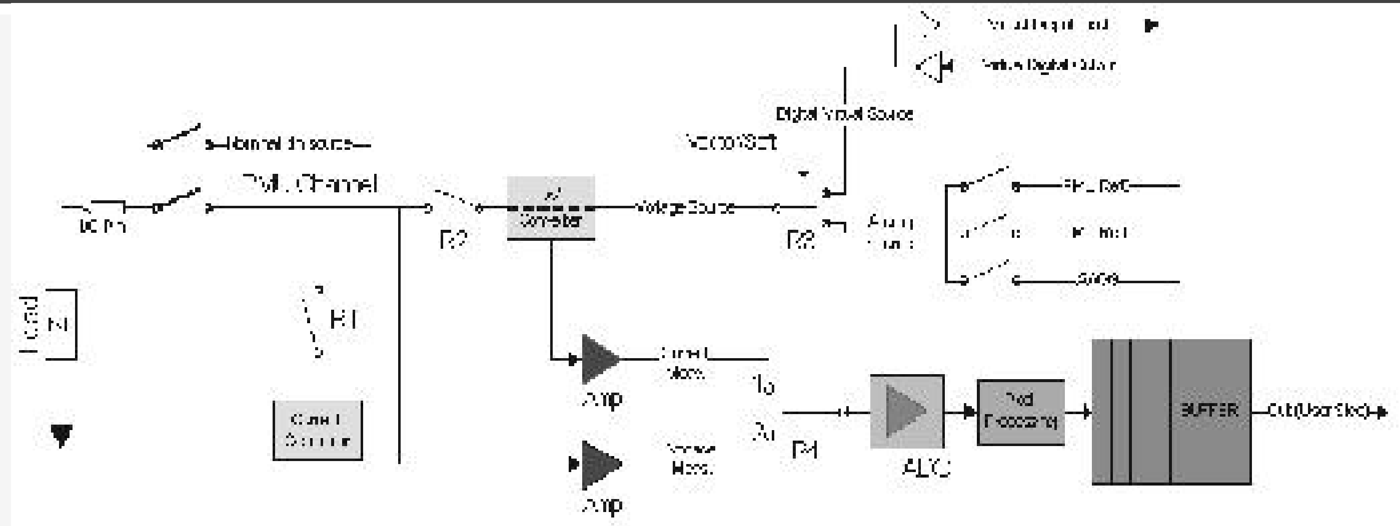
Digital Sequencer unit drives/stores the digital signals of the memory.

The integration between analog and digital resources allows easy synchronization of input generation ad output acquisition.



PMU reading performed in the middle of IOF waveform (optimal synchronization).

WP8: T8.1 RIFLE ATE PMU



PMU unit has been used to measure voltage on MUT data pins without any forcing operation.

Three parallel independent channels (one for each sensing pad).

Sample rate= 70 Mhz (14.3 ns resolution time).

Current and voltage measurement precision < 1 %.

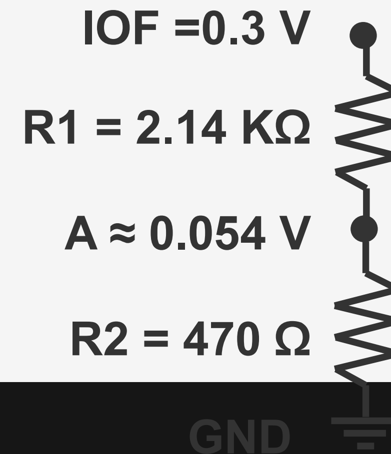
WP8: T8.1 RIFLE ATE Testing

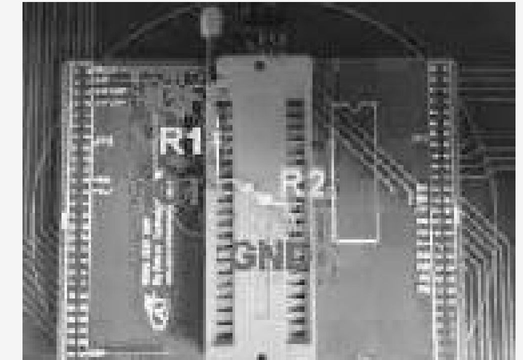
In order to check the measurement system stability 10.000 read operations have been performed using two test resistors (R1 = 2.14 kΩ, R2 = 470 Ω).

Results obtained on sensing pad IOT:

- Average read value = 63.135 mV
- Std. deviation = 0.137 mV

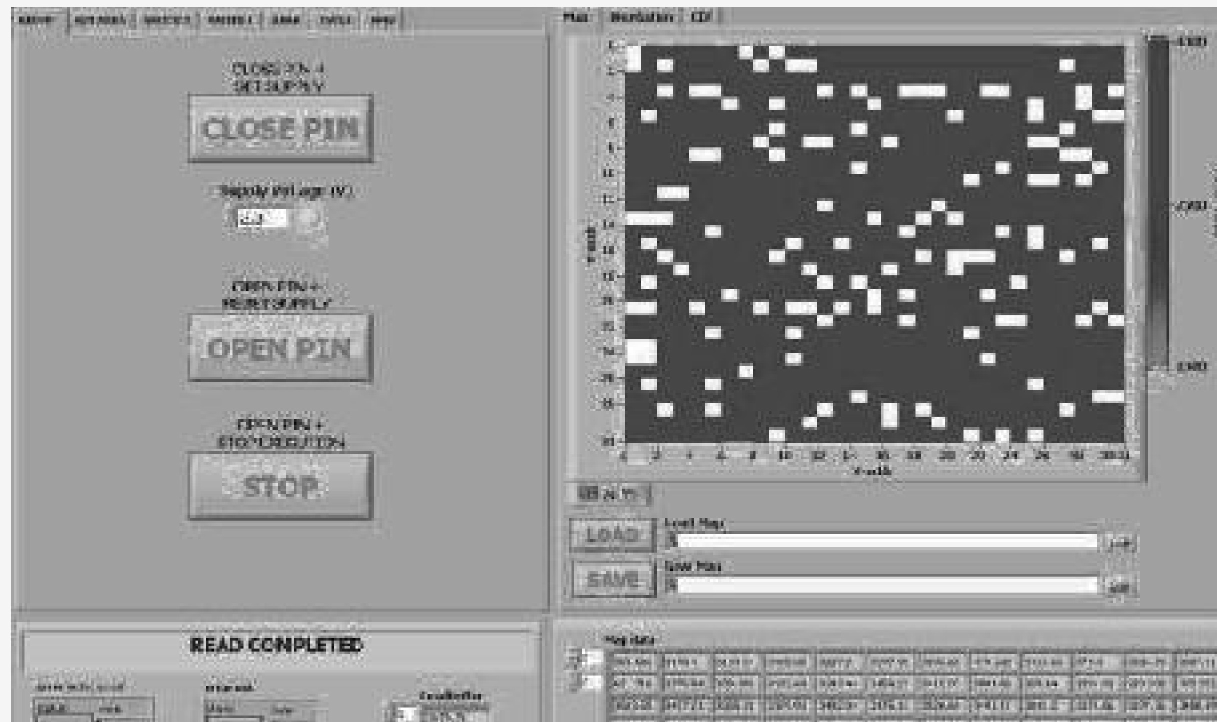
Similar results obtained on IOM, IOR sensing pads.





WP8: T8.1 RIFLE ATE Instrument Software

The Instrument software allows to execute single or cycled operations on single cells, cells subsets, array pages, blocks and full chip.



Results obtained in terms of read resistance maps and distributions can be graphically analyzed runtime.

WP8: T8.1 RIFLE ATE timing statistics

Timings required to perform standard reliability tests on full MRAM test array:

- Hysteresis analysis requires 25 write ’0’ and write ’1’ operations with different field line voltages, each one followed by a read operation.
- Read disturb analysis consist of 10.000 write ’0’ or write ’1’ operations.
- Endurance analysis consist of 500.000 consecutive write ’0’ and write ’1’ operations.

Test	Time [hours]	Test Parallelization
Hysteresis Analysis	1.27	No
Read Disturb (10k cycles)	3.4	No
Endurance (500k cycles)	160	Yes

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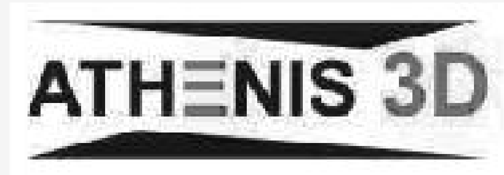
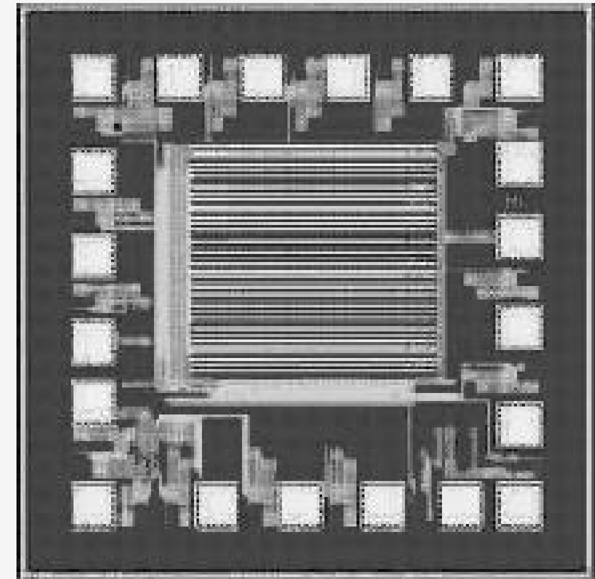
WP8: T8.2 Electrical characterization and statistical modeling of MRAM NVM



Start: M13

End: M28



MRAM preliminary test arrays

Objectives:

- Extensively investigate the embedded MRAM reliability through dedicated electrical characterization experiments (i.e., endurance, retention, disturbs, etc.)
- Develop models and new characterization methods as needed
- Provide statistical models for reliability assessment of the technology

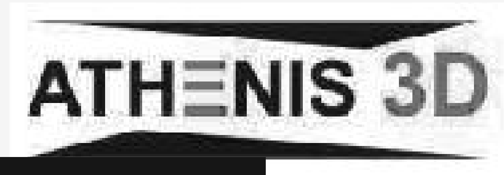
WP8: T8.2 Experimental Results on Low Temperature MRAM

V_{FORCE} = 1.4 V, T_{FORCE} = 500 ns.

V_{FORCE} voltage hysteresis measured in different cycling conditions, with $|V_{SWITCH}|$ = 5 V, T_{SWITCH} = 600 ns.

A resistance reduction can be observed due to cycling degradation.

WP8: T8.2 Experimental Results on Low Temperature MRAM



Cumula… and
W1 ope… V.

Left tails on the distributions appear during cycles due to degradation for a limited percentage of cells (below 3% after 500k cycles).

WP8: T8.2 Experimental Results on Low Temperature MRAM

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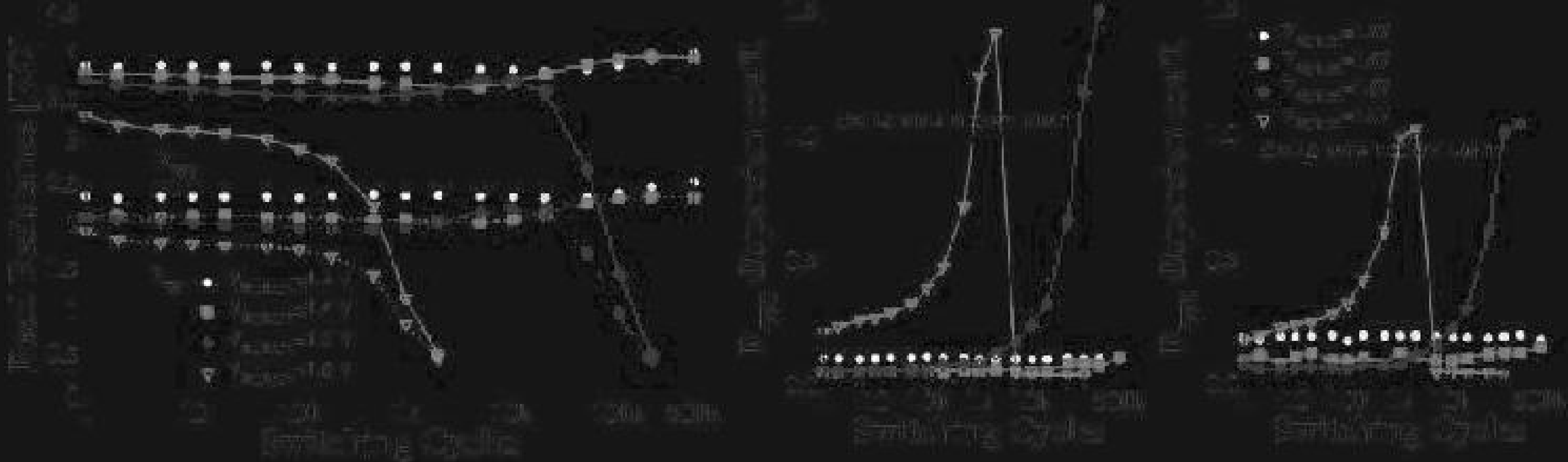


500k cycles have been performed with different V_{FORCE} values and $|V_{SWITCH}|$ = 5V, measuring R_{W0} and R_{W1} at different cycles.

R_{W0} and R_{W1} dispersion coefficients (i.e. standard deviation over mean value) show a rapid increase of their values before the breakdown.

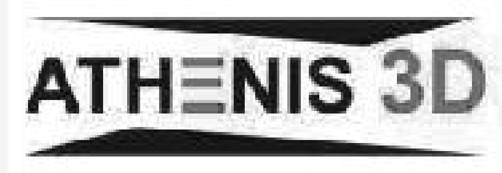
WP8: T8.2 Experimental Results on Low Temperature MRAM

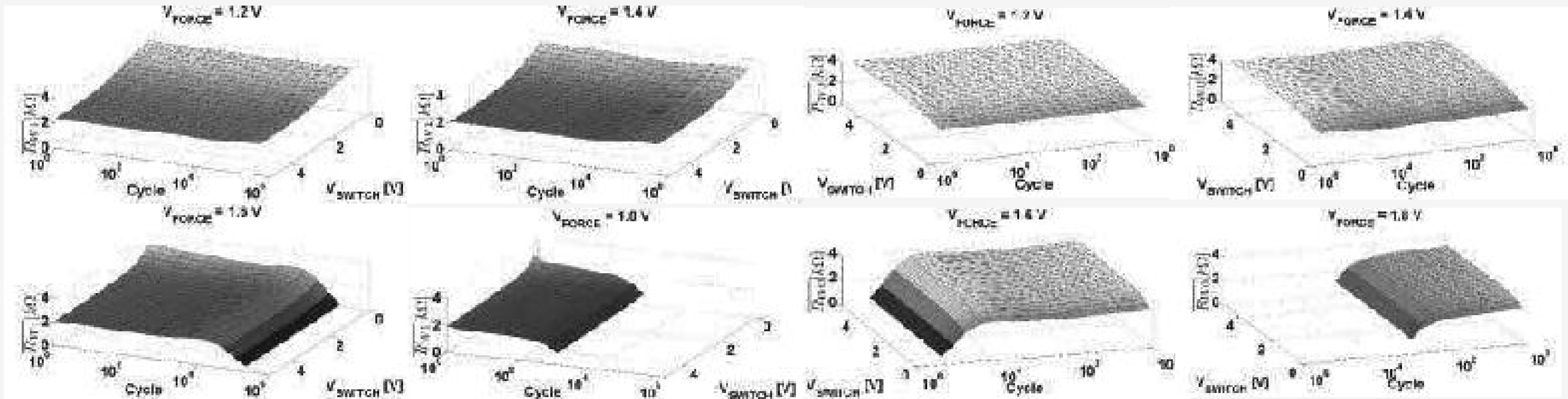
V_{W0} and V_{W1} are the switching voltages that allow obtaining a variation ΔR = 1k of the average measured resistance values.

The cumulative number of cells do not reach 1k because a limited number of cells do not reach, in switching, the assumed ΔR = 1k.

V_{FORCE} = 1.4V shows the highest cumulative number of cells reaching the requested resistance variation ΔR = 1k.

WP8: T8.2 Experimental Results on Low Temperature MRAM





R_{W1} R_{W0}

R_{W0} and R_{W1} are shown to depend on V_{FORCE}, V_{SWITCH} and cycling: the relationship between these parameters has been analyzed through 3D plots for different V_{FORCE} conditions.

Using too high heating voltages (i.e. V_{FORCE} 1.6V) results in a shorter lifetime, independently from V_{SWITCH}.

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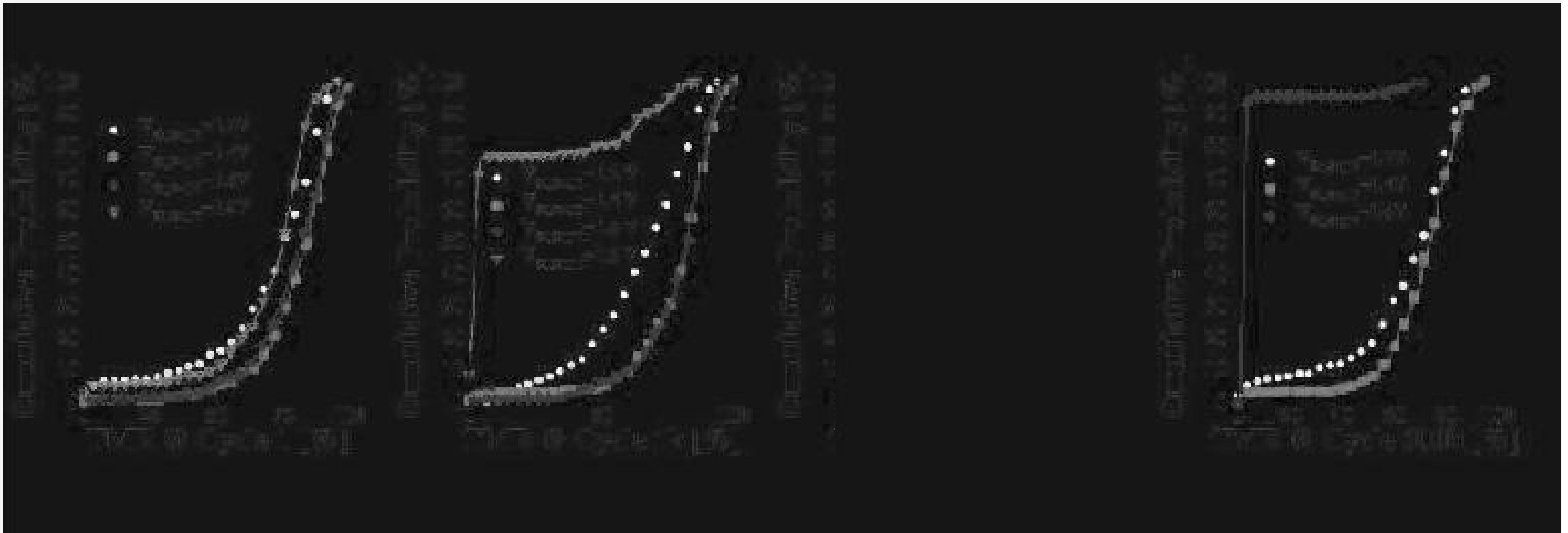
WP8: T8.2 Experimental Results on Low Temperature MRAM

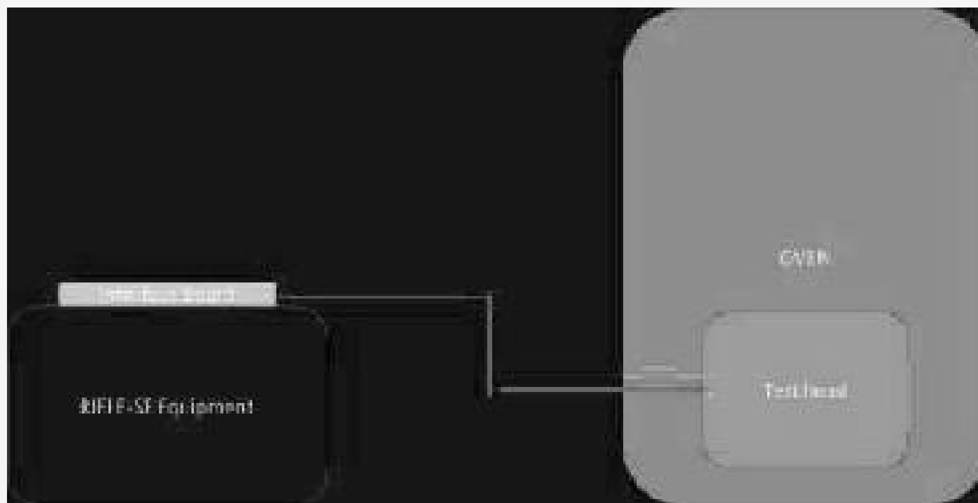


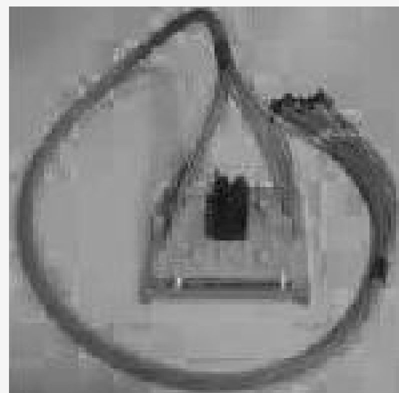
TMR evolution during cycling has been analyzed in terms of cumulative probability distributions.

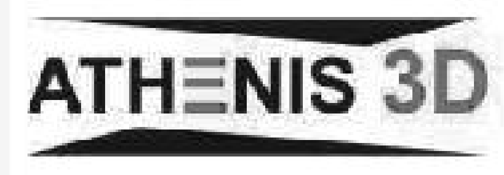
No relevant variations can be observed on TMR until the cell breakdown is reached.

WP8: T8.2 Experimental setup for High Temperature TAS-MRAM testing

- After the first experiments conducted at room temperature on a packaged device, Active Technologies supported the evolution of the system in order to allow the next tests in a temperature range from 25° C to 200 ° C
- To allow the placement of the test head into an oven, the interconnection between the test head and the ATE made by cables as shown in Figures

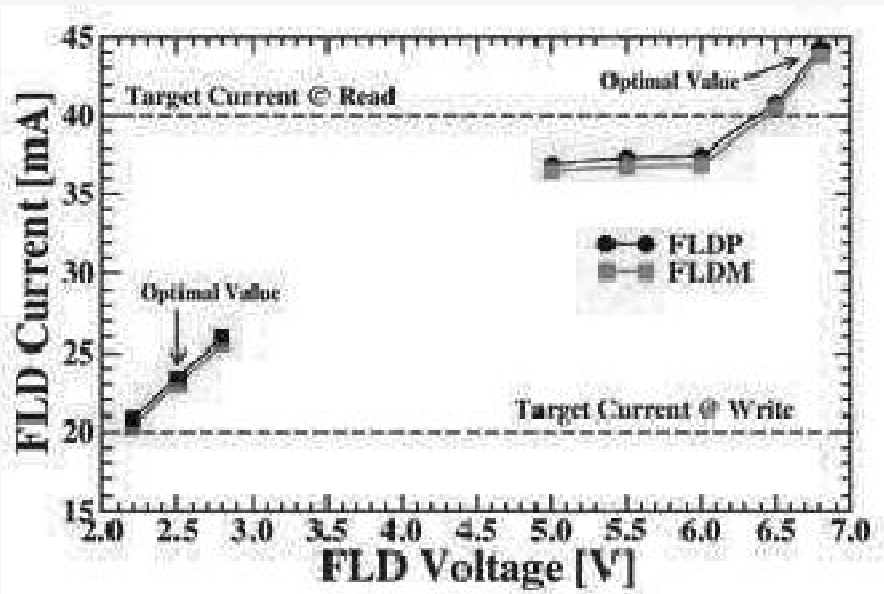






WP8: T8.2 Optimal High Temperature TAS-MRAM switching parameters

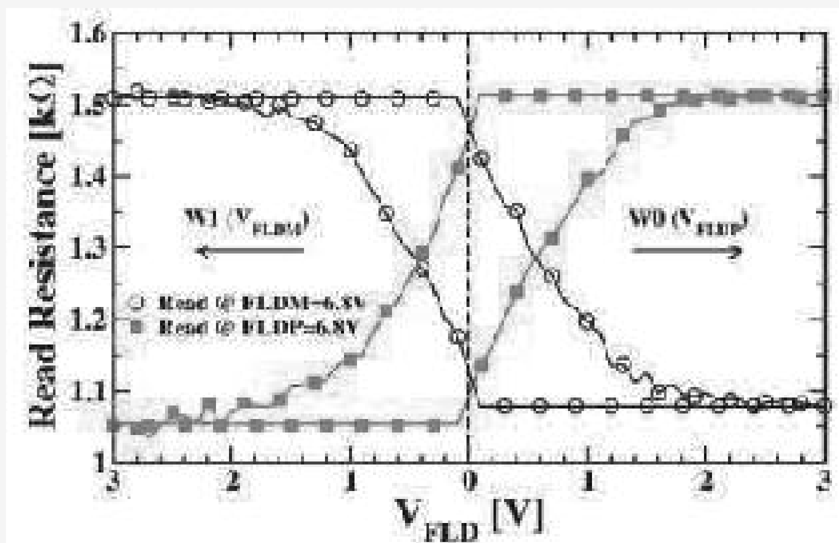
- The target (requested) values and the optimal values (that allows obtaining the best performances, extracted through the electrical characterization) for the HV TAS-MRAM NVM technology are indicated
- A resume of the read and write parameters that allowed obtaining the best performances is reported in Table

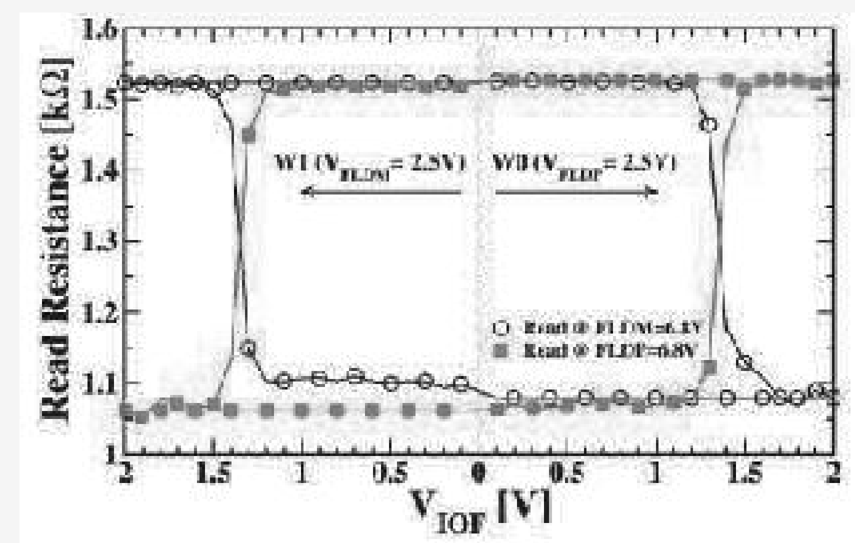


Operation	V[illegible]	T[illegible]	T[illegible]	V[illegible]	T[illegible]	T[illegible]	V[illegible]
Read	0.3 V	50 us	5 us	6.0 V	70us	1us	6.5 V
Write '0' (FLDP)	1.6 V	500 ns	100 ns	2.5 V	700 ns	100 ns	6.5 V
Write '1' (FLDM)	1.8 V	500 ns	100 ns	2.5 V	700 ns	100 ns	8.5 V

WP8: T8.2 High Temperature TAS-MRAM hysteresis characterization

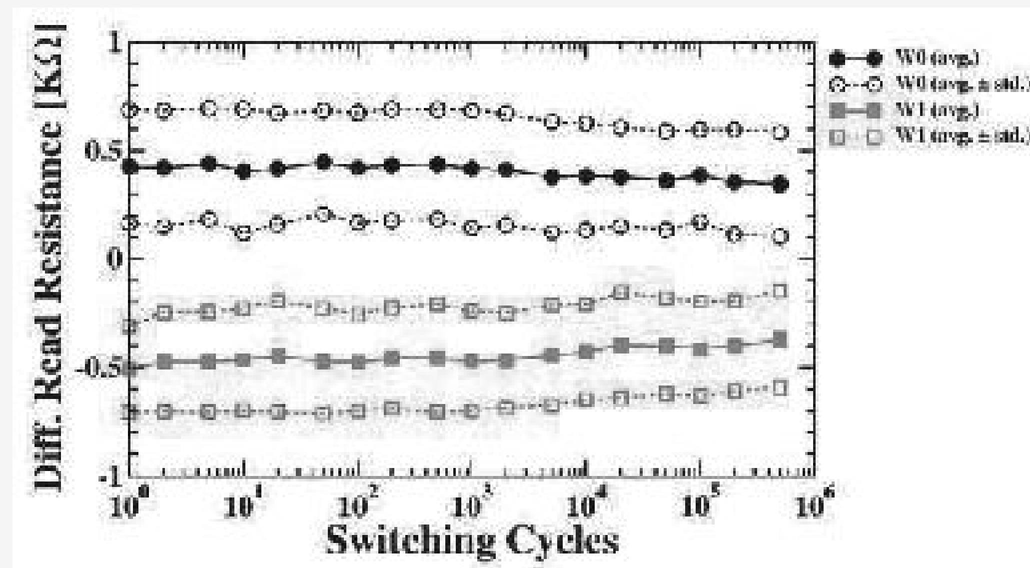
- To evaluate the impact of heating (VIOF) and switching (VFLD) voltages on write operations, a preliminary hysteresis analysis of both parameters has been performed on fresh devices
- The field line voltage hysteresis was measured by applying write pulses with VPULSE,IOF=1.6, TPULSE,IOF=500ns, VPULSE,FLD increased from 0.1 to 3V with VSTEP= 0.1V, TPULSE,FLD=700ns and TRISE/FALL=100ns for both pulses
- The IOF line voltage hysteresis was measured by applying write pulses with VPULSE,IOF increased from 0.1V to 2V with VSTEP=0.1V, TPULSE,IOF=500ns, VPULSE,FLD increased from 0.1V to 3V with VSTEP=0.1V, TPULSE,FLD=700ns and TRISE/FALL=100ns for both pulses

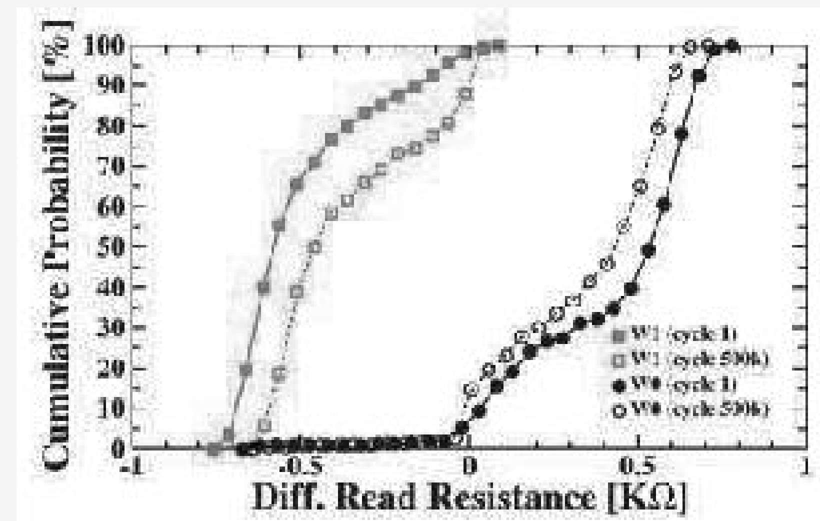




WP8: T8.2 High Temperature TAS-MRAM endurance characterization

- To evaluate the cells performance and reliability during cycling and the effect of the cell degradation, 500k Write ‘0’ and Write ‘1’ operations have been performed
- The differential resistance, calculated as Rread,FLDP-Rread,FLDM is difference between the read resistances measured when the field line voltage is applied on FLDP and FLDM, respectively. The average values and the standard deviation of the differential read resistances calculated after Write ‘0’ and Write ‘1’ operations during 500k cycles and the cumulative distributions of the differential read resistances obtained after Write ‘0’ and Write ‘1’ operations, at cycle 1 and after 500k cycles are reported showing high reliability for automotive applications





WP8: T8.2 High Temperature TAS-MRAM retention characterization

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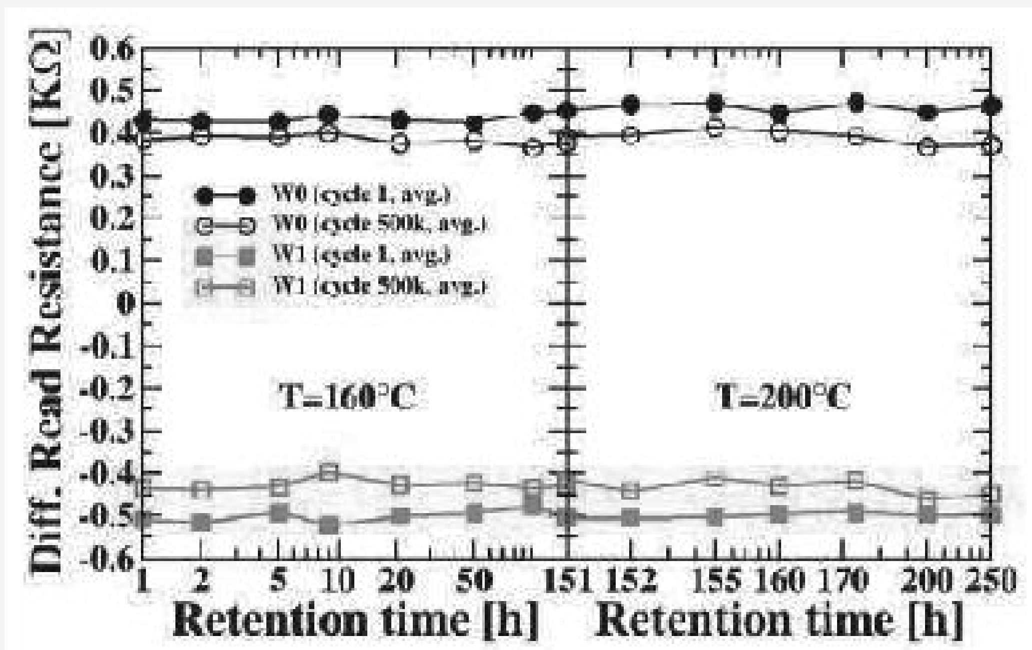
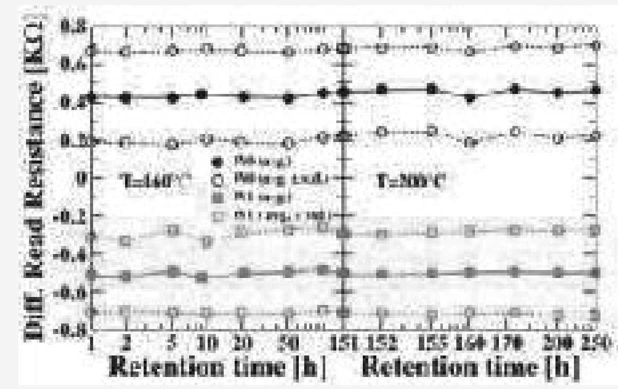
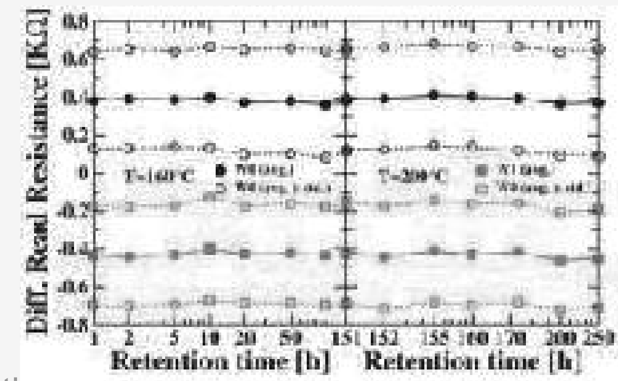
- Measurements have been performed to evaluate the data retention degradation by baking ceramic packaged test chips with both fresh and cycled devices at 160° C for 150 hours and then at 200° C for 100 hours. Cumulative distributions of Read Resistances measured after Write ‘0’ and Write ‘1’, before and after the retention tests on fresh and cycled devices are reported, respectively
- The temperature tests show no relevant impact on the measured distributions



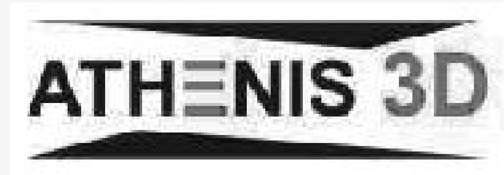
Fresh





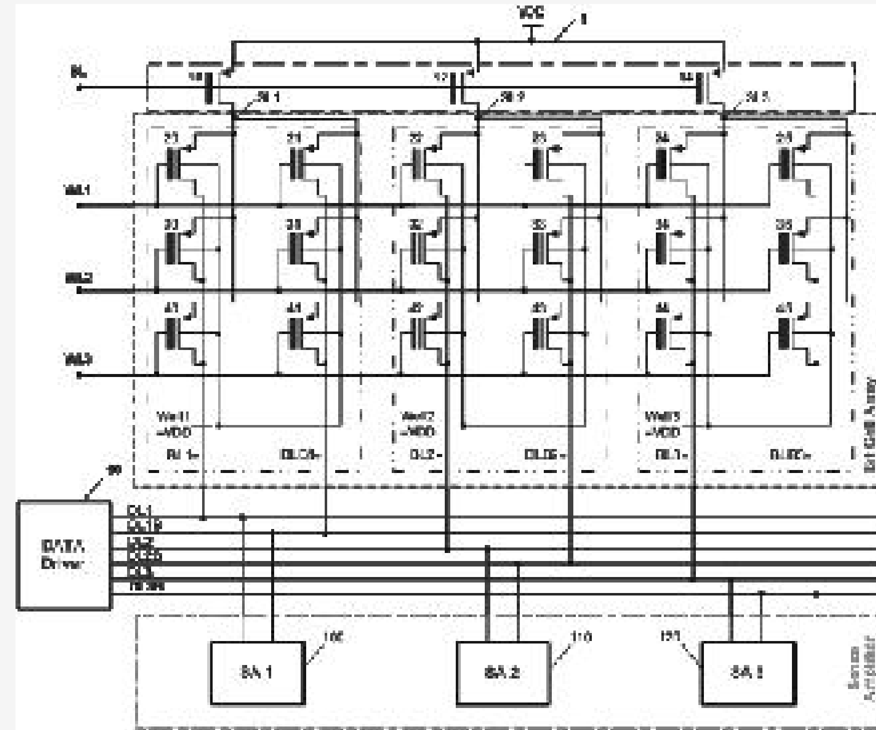
Cycled

WP8: T8.3 Reliability benchmark MRAM vs SimpleEE



Start: M25

End: M30

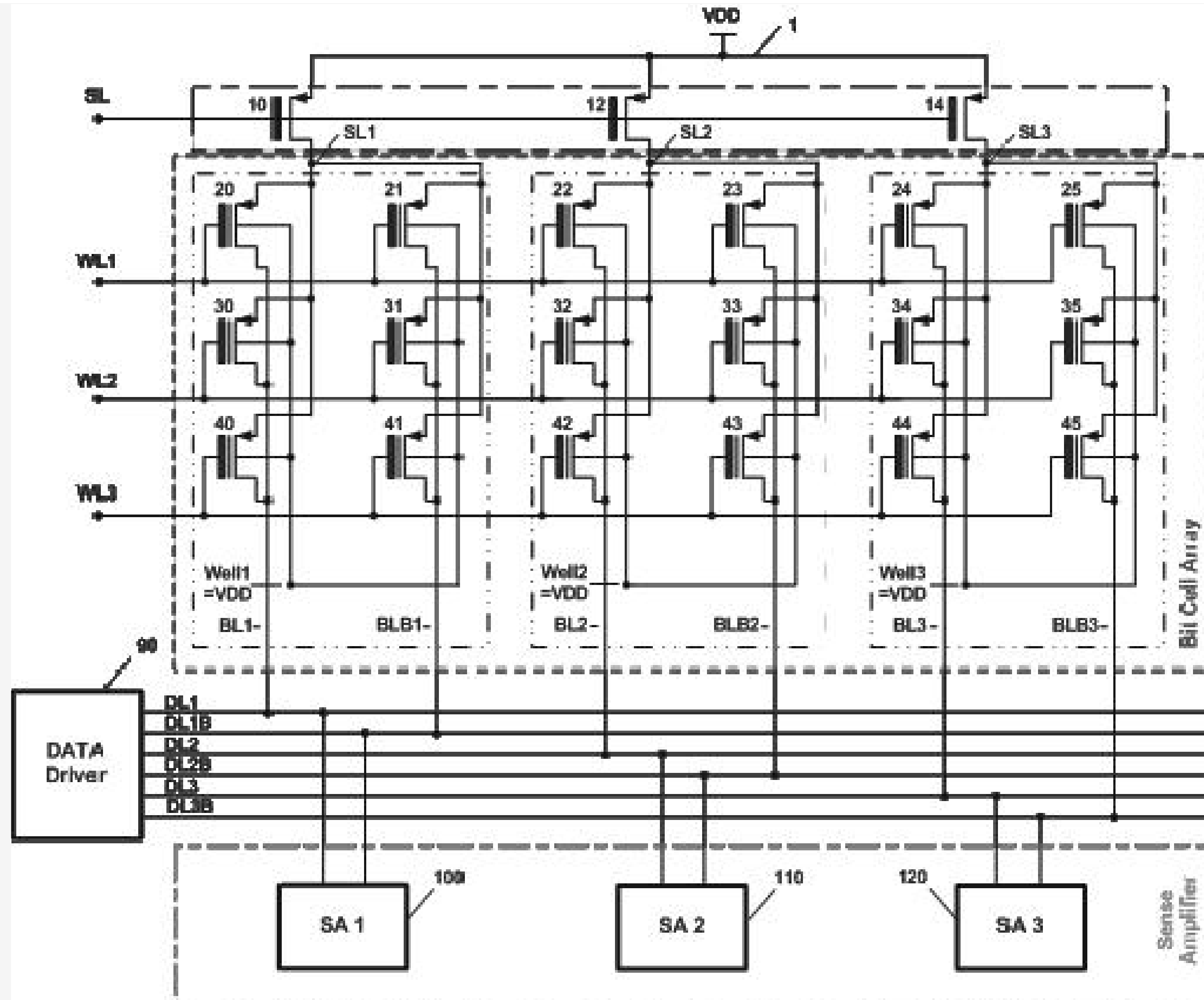


New SimpleEE robust design

Objectives:

- Provide a benchmark between the NVM module in ATHENIS_3D SoC vs. the SimpleEE module exploited in ATHENIS proposal
- Thoroughly characterize the new simpleEE robust design
- Benchmark the NVM concepts together in order to assess the solidity of the proposed integration approach

WP8: T8.3 Activities on H35 NVM module



The testing of a more robust design of the C35 SimpleEE has been introduced in the activities of the WP8

H35 4kX16 bits arranged in a 2 cells per bit paradigm

WP8: T8.3 Technology comparison

	SimpleEE family	TAS-MRAM family
Base Technology	AMS 0.35µm full-CMOS	TowerJazz CMOS + Crocus MTJ
Array Size	4Kx16	1K
Transistor per Cell	3 (Floating gate + SSTs)	1
Technology variants	SimpleEE standard + Differential SimpleEE (robust)	Fixed Reference (Low T) + Self Reference (High T)
Writing Capabilities	DiNOR-like with 16 bits	Page/Block addressable for parallel testing or bit-alterable
Reading Capabilities	EEPROM Standard (SimpleEE) + Differential mode (robust)	SRAM-like
Power Supplies	VDD (CORE), VPP (for Program/Erase)	VDD (CORE), IOF (Read/Write), IOFLDP, IOFLDM (Read/Write for SR, only Write for FR)

WP8: T8.3 Write operation comparison

	SimpleEE technology
Power Supply	3.3 V
Vpp exploited	From 9 V up to 14 V in steps of 1 V (each step takes 200 μs)
Optimal Programmed Value	27 μA (using Vpp 13 V for 4 ms)
Optimal Erase State Value	1 μA (using Vpp 13 V for 4 ms)

MRAM technology

	Low Temperature technology	High Temperature technology
Power Supply	3.6 V	5 V
VFORCE	0 V up to 2 V	0 V up to 2 V
VSWITCH	From -5 V up to 5 V	From -5 V up to 5 V
Optimal Write 0 State Value	3700 Ω	1500 Ω
Optimal Write 1 State Value	2100 Ω	1000 Ω

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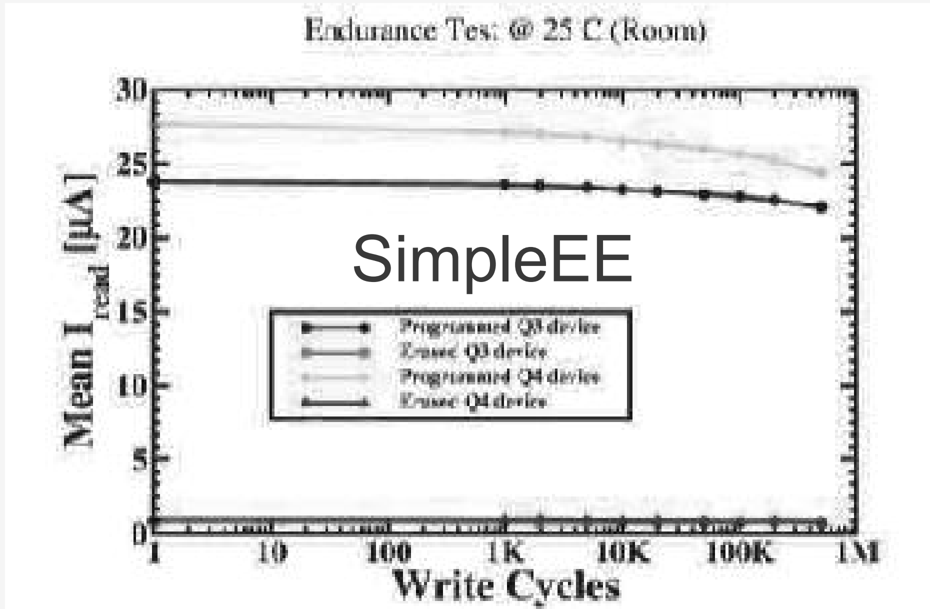
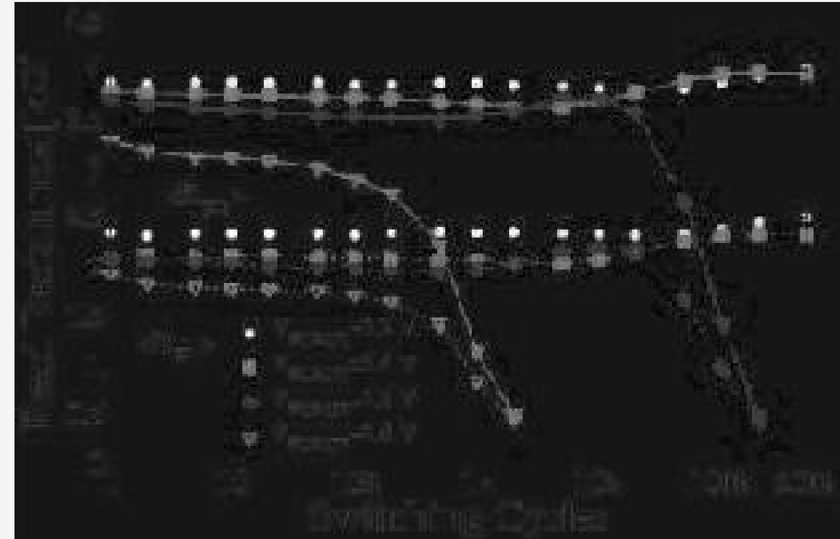
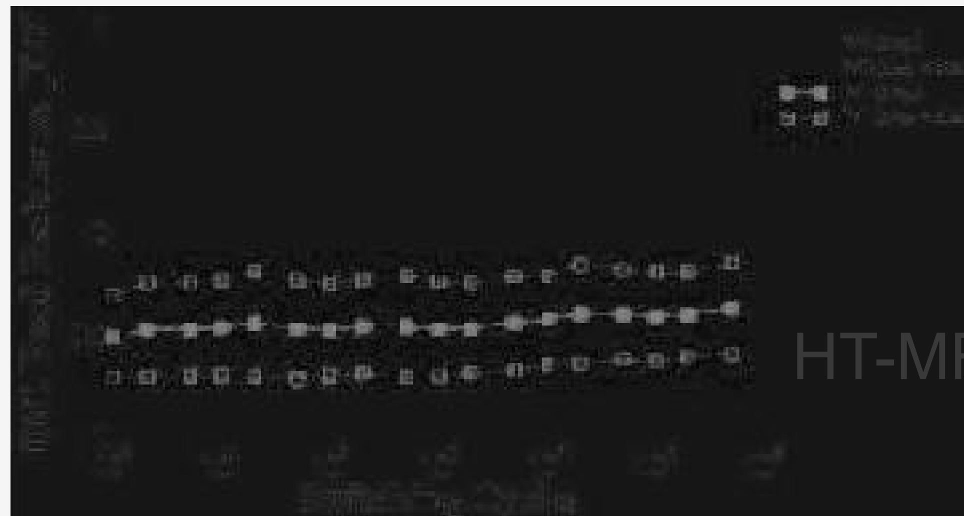
WP8: T8.3 Endurance comparison (500k cycles)



SimpleEE



LT-MRAM

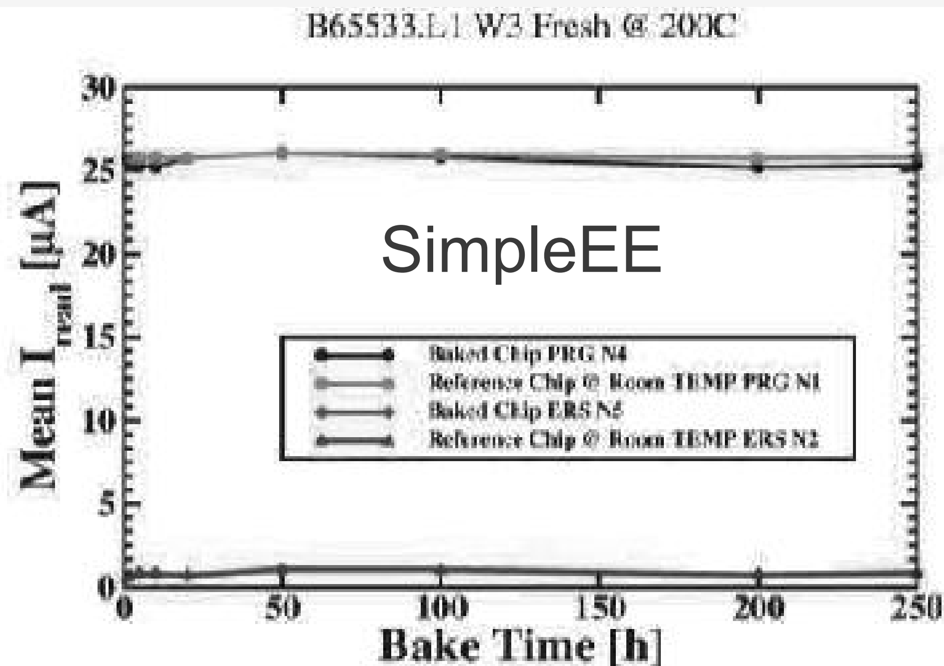


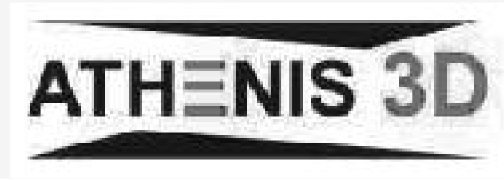
HT-MRAM

All tested technologies are able to withstand 500k cycles according to automotive standards

WP8: T8.3 Data retention comparison

	SimpleEE	TAS-MRAM
Testing Temperature	100° C, 150° C, 200° C, and 250° C	160° C and 200° C
Tested concepts	Standard and differential	Self-Reference (SR) only
Test Typology	Stepped stress	Stepped stress
Power Supply during Read	3.3 V	5 V
Retention Test Duration	1000h	250 h (100h @ 200° C)
Array status for Retention	Full Programmed, Full Erased, Checkerboard pattern	Write 0 blocks and Write 1 blocks
Retention Failures?	No	No





Task 8.5: Physical Reliability Modeling of NVMs

Start: M25

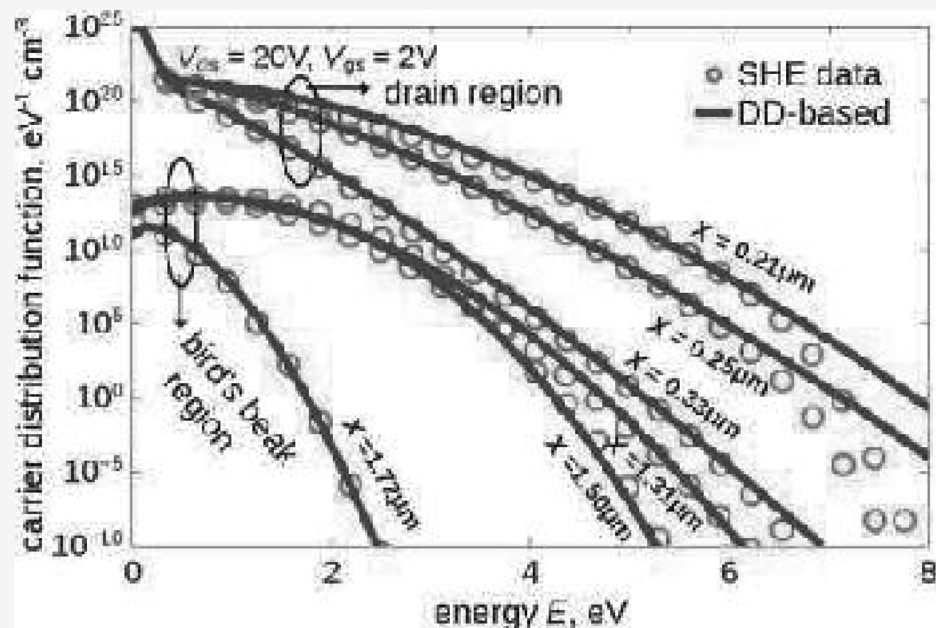
End: M32

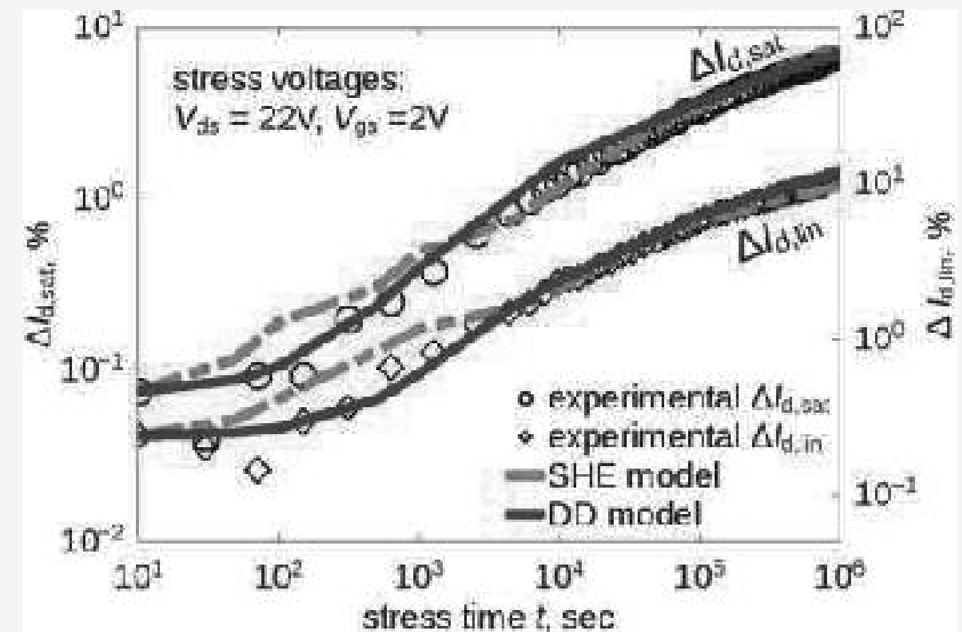
Analytic Hot-Carrier Degradation Model

Simplified techniques of the BTE solution

- Drift-diffusion (DD) model
- Energy transport model

- Is the drift-diffusion scheme applicable?
  - our DD based model captures HCD in LDMOS devices[1,2]
  - fails for planar MOSFETs with channels shorter 1.5μm[3,4]





[1]P. Sharma *et al.*, IEEE TED 2015 [2]P. Sharma *et al*, SISPAD 2015
[3]S. Tyaginov *et al.*, ESSDERC 2011 [4]M. Jech *et al.*, J. JAP 2016

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Analytic Hot-Carrier Degradation Model

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What about scaled devices?

Electron-electron scattering (EES) must be considered[1-3]

populates high energy fraction

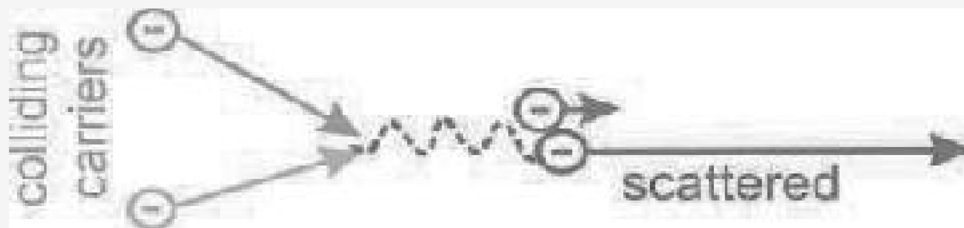
changes the DF shape

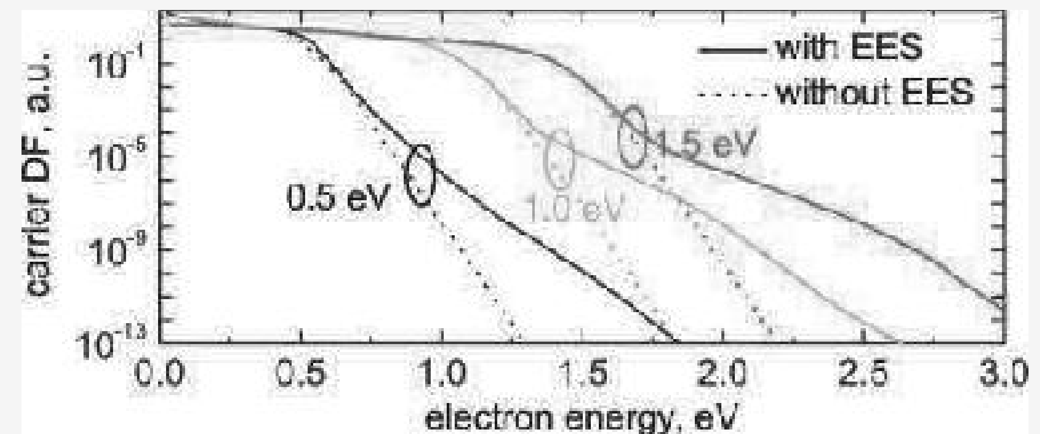
enhances HCD

Requirements for the extended model

represents DF obtained with ViennaSHE

represents $\Delta I_{\mathrm{d,lin}}(t)$





[1]P.A. Childs, C.C.C. Leung, JAP, 1996 [2]S.Rauch *et al.*, IEEE EDL 1998
[3]S.Tyaginov *et al.*, J. JAP 2015

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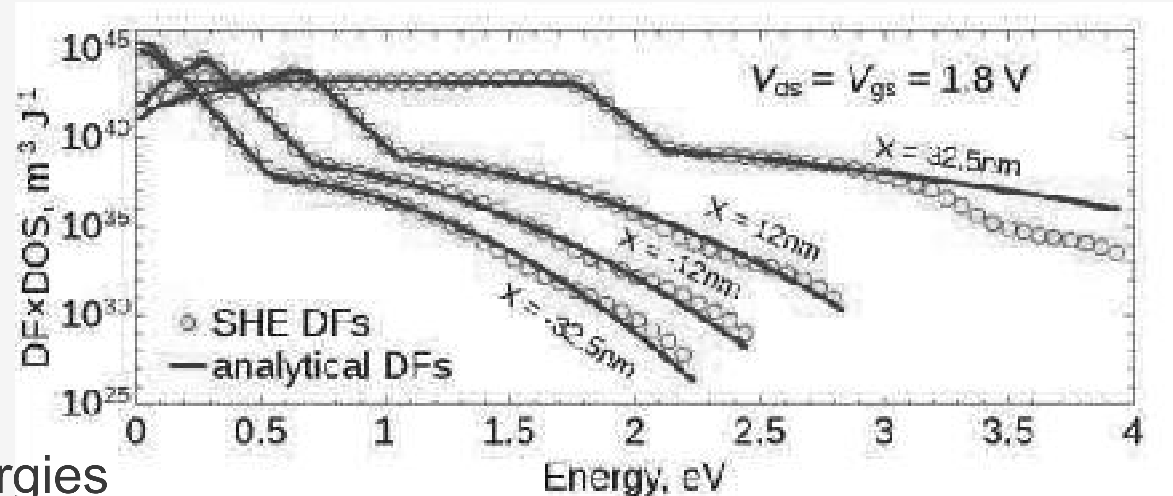
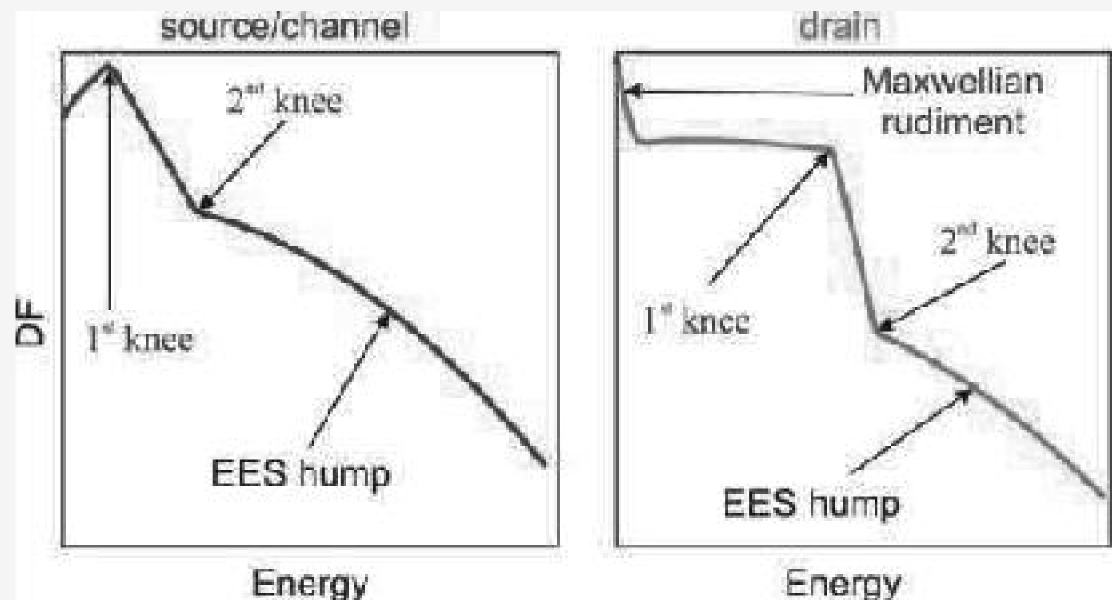
Analytic Hot-Carrier Degradation Model

Peculiarities of the DF

- Different shapes
- Source/channel DFs
  - maximum at $\varepsilon_{k,1}$
  - $\varepsilon_{k,1}$ – first knee energy
- Drain DFs
  - plateau at moderate energies
  - plateau and at $\varepsilon_{k,1}$
- Electron-electron scattering
  - hump at high energies
  - observed at $\varepsilon_{k,2}$





Analytic Hot-Carrier Degradation Model

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The DD-based version of the model

Evaluates the field $F(x)$, the mobility $\mu(x)$, and the concentration $n(x)$

The carrier temperature is obtained: $T_n = T_L + \frac{2}{3}\frac{q}{k_B}\tau\mu F^2$

The carrier DF[1]:

$$f(E) = A\exp\left[-\left(\frac{E}{E_{\mathrm{ref}}}\right)^{\mathrm{b}}\right] + C\exp\left[-\frac{E}{k_{\mathrm{B}}T_{\mathrm{L}}}\right]$$

A, *C*, *and* E_{ref} are found as:

$$\int_0^\infty f(E)g(E)\mathrm{d}E = n$$

$$\int_0^\infty Ef(E)g(E)\mathrm{d}E = \frac{3}{2}nk_{\mathrm{B}}T_{\mathrm{n}}$$

$$\int_0^\infty f(E)\mathrm{d}E = 1$$

[1] T. Grasser *et al.* APL 2002

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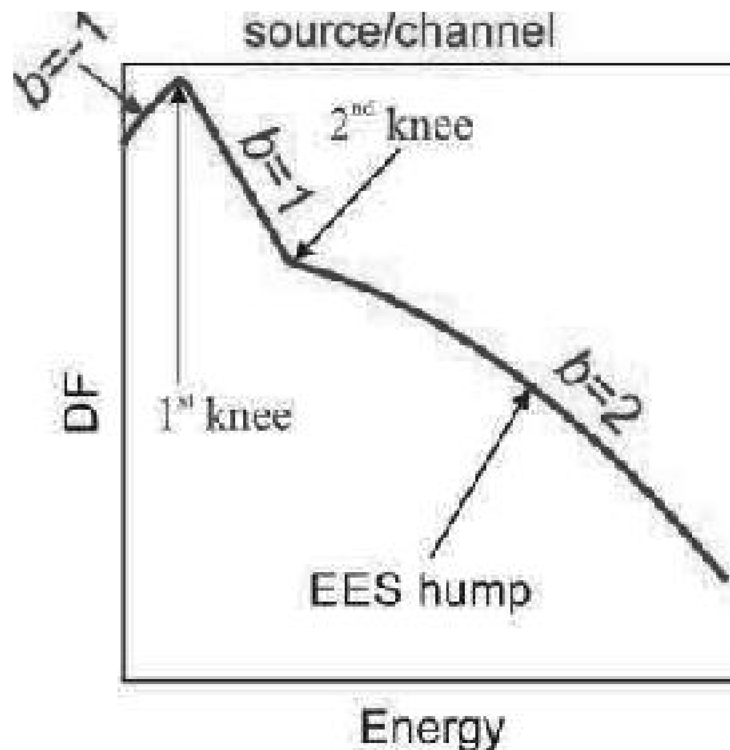
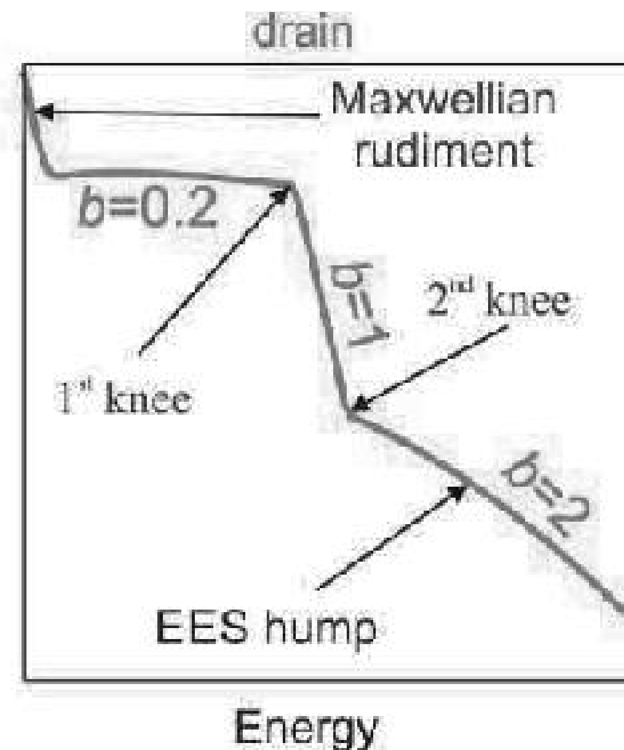
Parameterization of the DF

$$f(E) = A\exp\left[-\left(\frac{E}{E_{\mathrm{ref}}}\right)^{\mathrm{b}}\right] + C\exp\left[-\frac{E}{k_{\mathrm{B}}T_{\mathrm{L}}}\right]$$



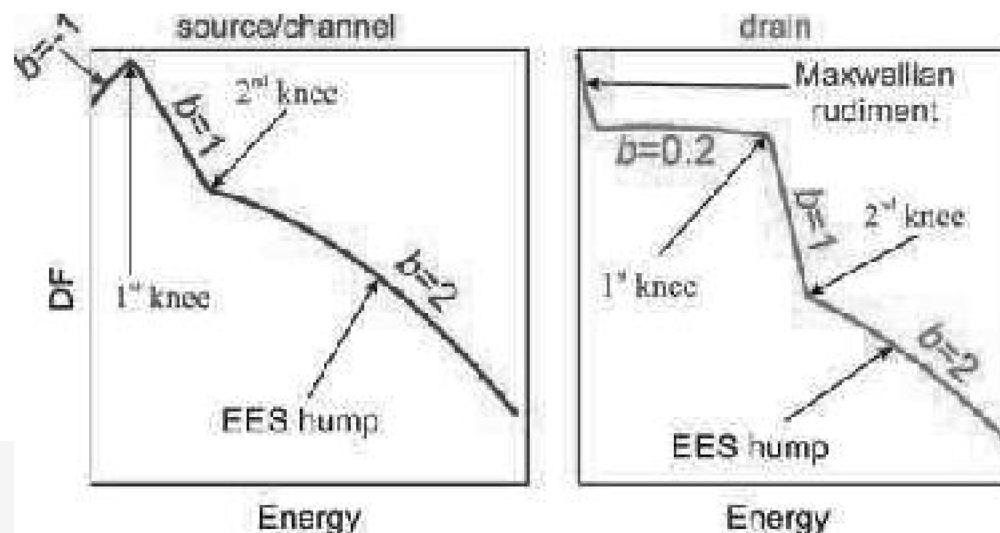


The general procedure

$$f(E) = A\exp\left[-\left(\frac{E}{E_{\mathrm{ref}}}\right)^{\mathrm{b}}\right] + C\exp\left[-\frac{E}{k_{\mathrm{B}}T_{\mathrm{L}}}\right] \quad (1)$$

$$\varepsilon_{\mathrm{k,1}} = \alpha\exp\left[\beta - (\gamma - \delta F)^{1/2}\right] \quad (2)$$

$$r_{\mathrm{EES}} = r_{\mathrm{ii}} + r_{\mathrm{opt/abs}} + r_{\mathrm{opt/emi}} + r_{\mathrm{acc}} \quad (3)$$



Calculate DF without EES from (1)

↓

Evaluate $\varepsilon_{k,1}$ using (2)

↓

Find $\varepsilon_{k,2}$ using the scattering rate balance, (3)

↓

Calculate new DF changing 'b' at $\varepsilon_{k,1}$ and $\varepsilon_{k,2}$, see Fig. 1

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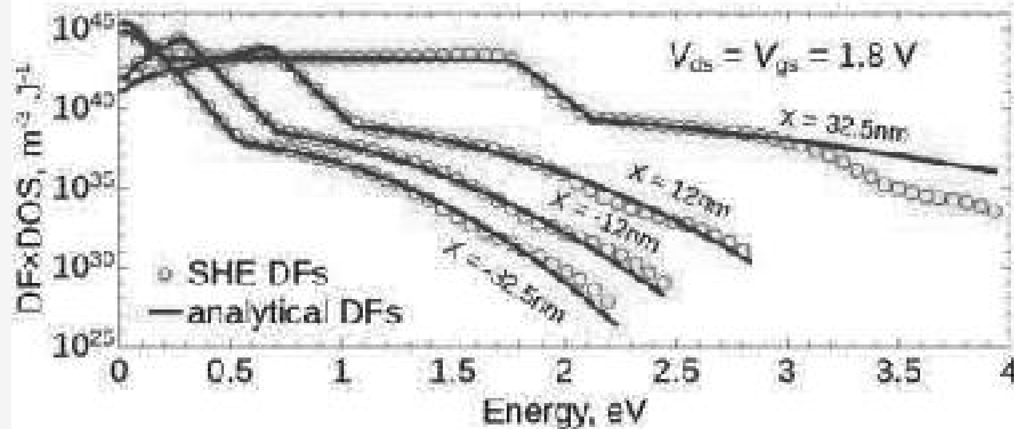
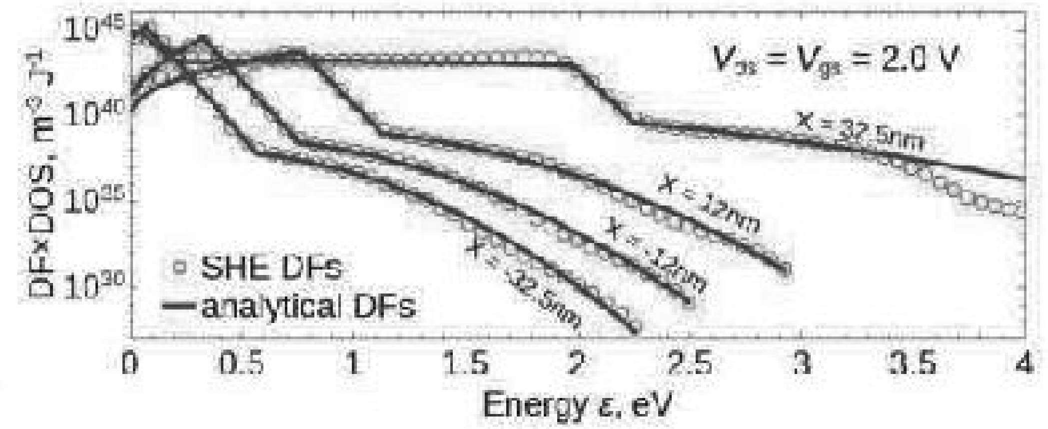
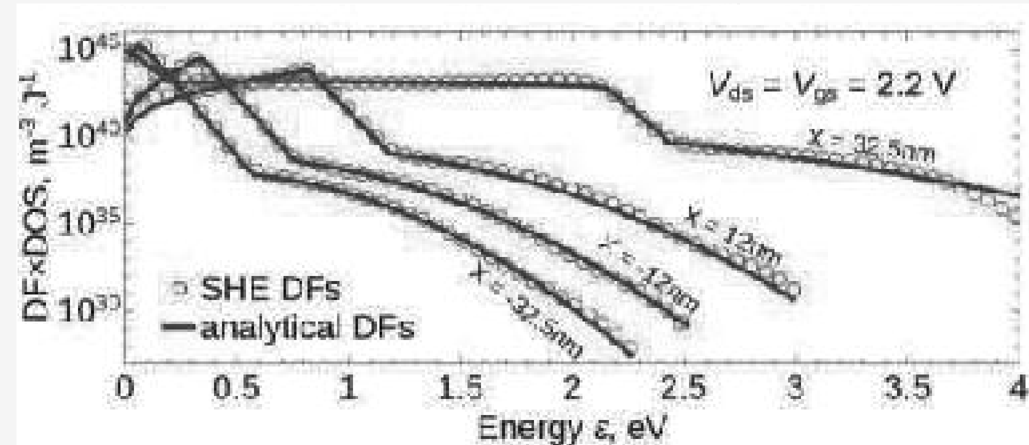
Analytic Hot-Carrier Degradation Model

Distribution functions

- Excellent agreement between ViennaSHE and DD-based model
- Slight discrepancy is visible after $\varepsilon_{k,2}$





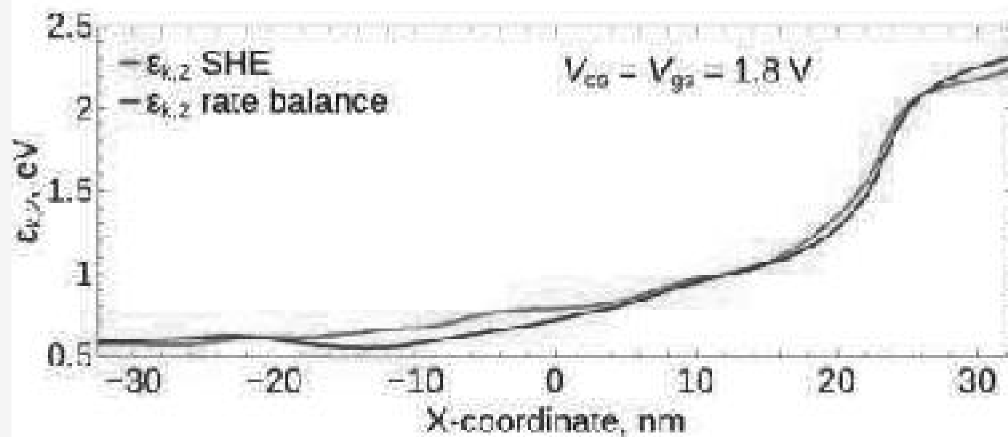


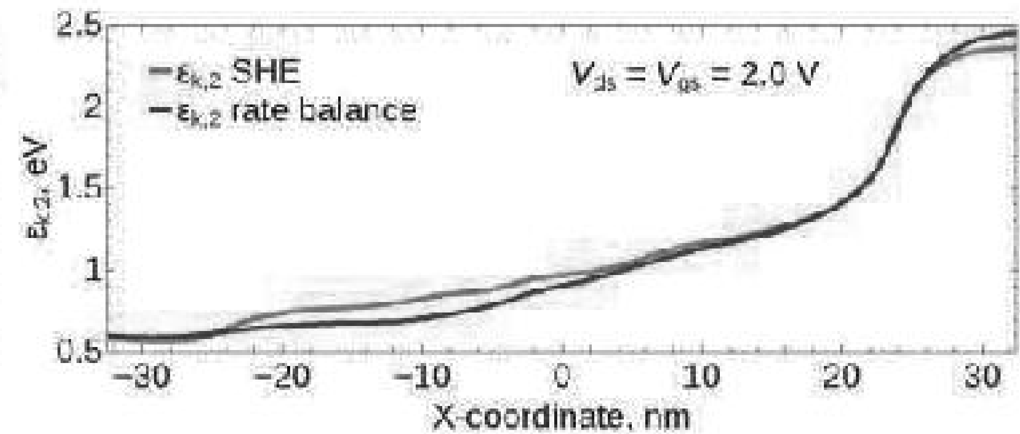
Analytic Hot-Carrier Degradation Model

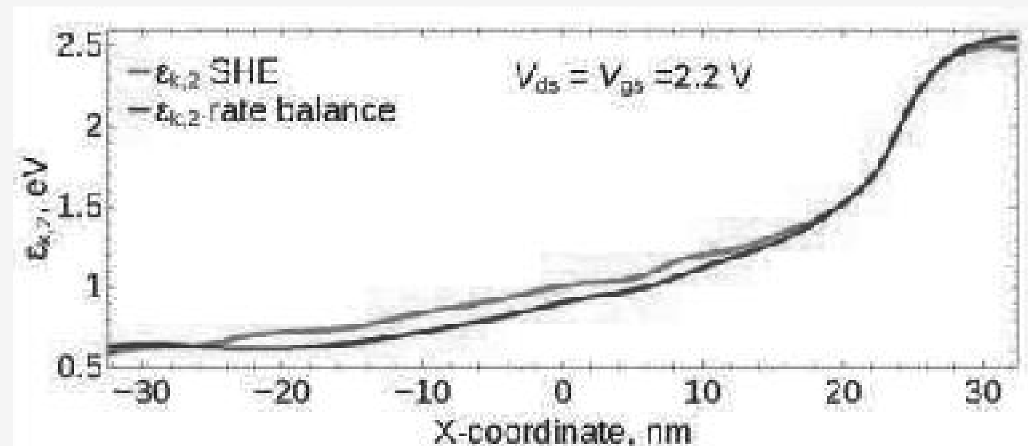
Knee energies $\varepsilon_{k,2}$

Excellent agreement between ViennaSHE and DD-based model

This is true for the entire device







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HCD model validation

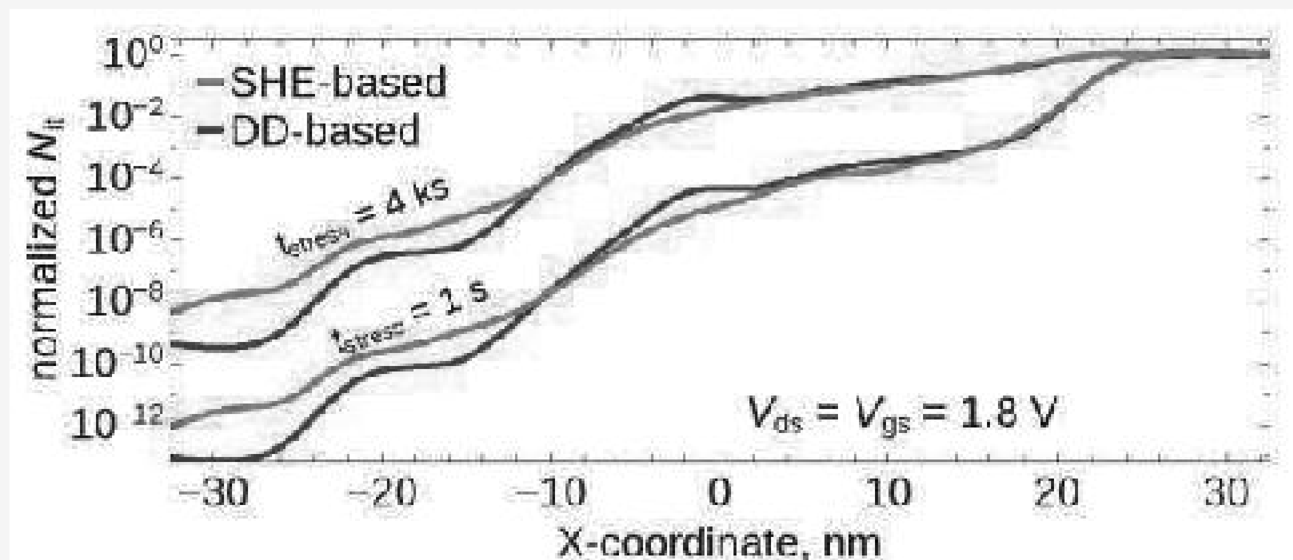
SiON nMOSFET with L_G = 65nm

Stress at $V_{gs} = V_{ds}$ = 1.8, 2.0, and 2.2V for ~8ks

The linear drain current change $\Delta I_{d,lin}(t)$ is monitored

Normalized $N_{it}(x)$ profiles

- ViennaSHE based results vs. drift-diffusion based results
- some discrepancy at x = -5nm
- N_{it} values dropped by 4 orders → no error in $\Delta I_{d,lin}(t)$ traces

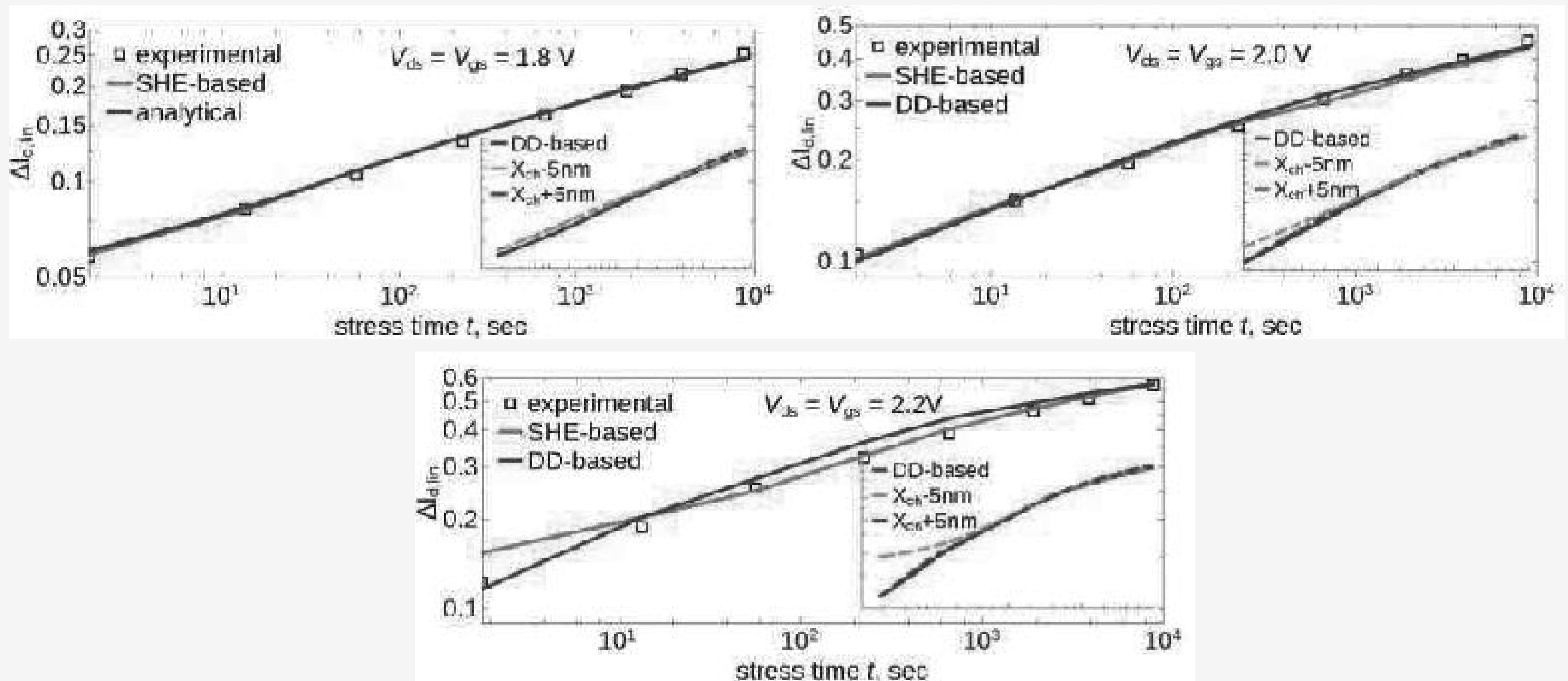


Analytic Hot-Carrier Degradation Model

Linear drain current changes $\Delta I_{d,lin}(t)$

Results of two version of the model vs. experimental data

Agreement is very good!



WP8: T8.5 Conclusions

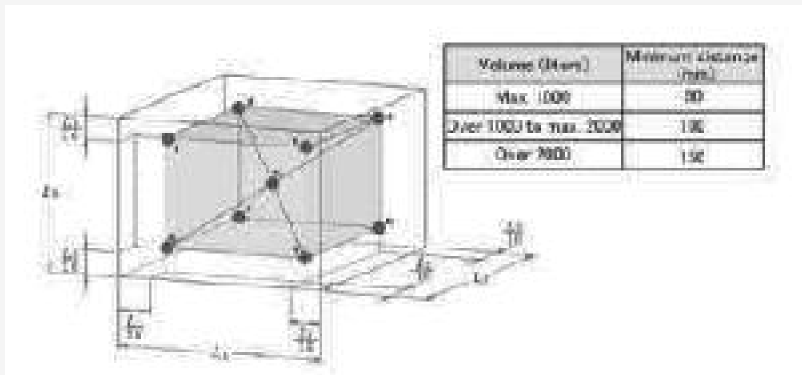
The drift-diffusion based analytical HCD mode can properly represent:

- carrier distribution functions
- interface state density profiles
- degradation $\Delta I_{d,lin}(t)$ traces

Reliability Test on TSV

- TCY up to +250C, way beyond existing
- HTS up to +300C

- TCY system build by ESPEC Japan
- 1st delivered to EU, range -77C/+305C
- Calibration and Uncertainty according ISO 17025 standards
- Material incompatibility solvedC
- Calibration passed range -70C/+300C

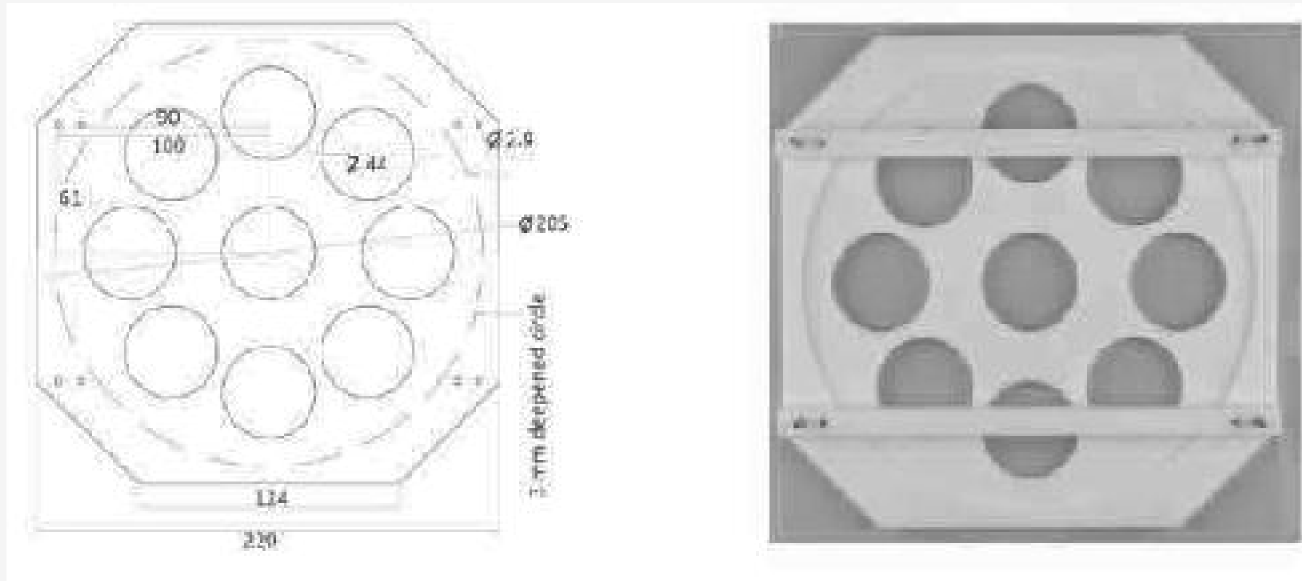


Volume (liters)	Minimum distance (mm)
Max. 1000	50
Over 1000 to max. 2000	100
Over 2000	150

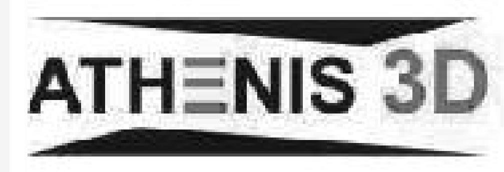
Reliability Test on TSV

- TCY up to +250C, way beyond existing
- HTS up to +300C

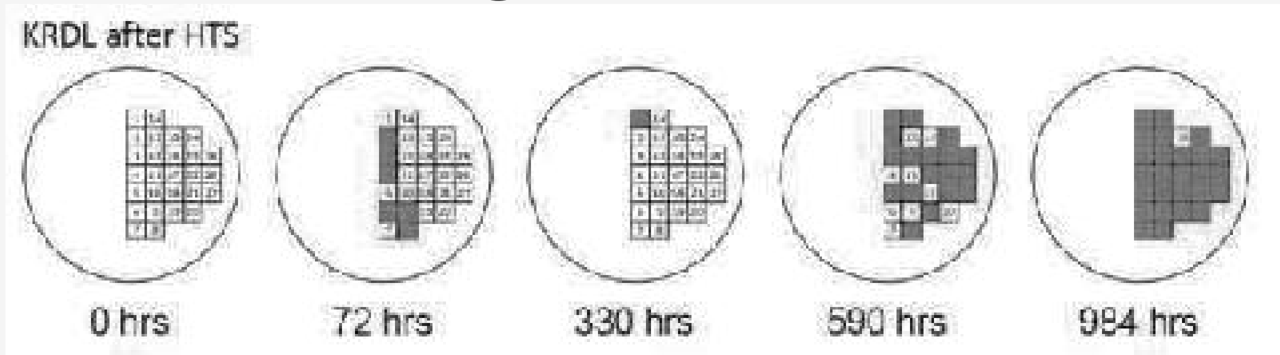
- Wafer level test of TSV wafers required dedicated handling tools
- E-test of wafer stack with semi-automatic prober



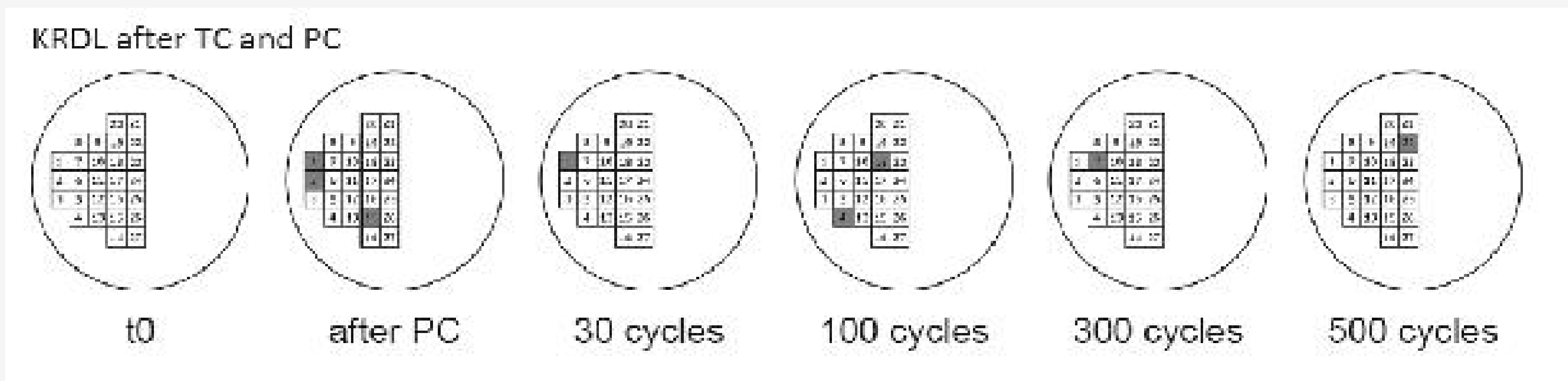
Reliability Test on 3DT1 W06 TSV



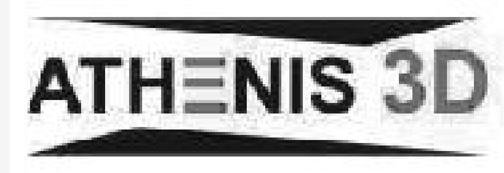
- HTS, 1000 hours @ +200C HTS test



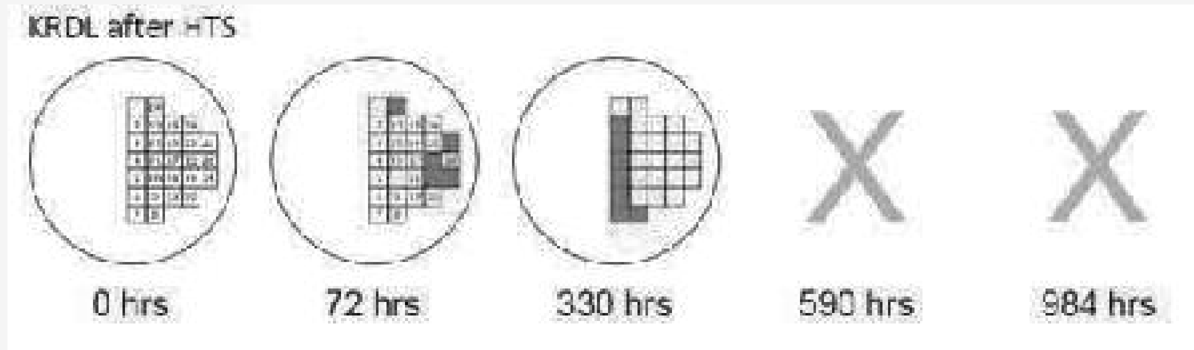
- TCY, 500 cycles after precon, range -65/+200C



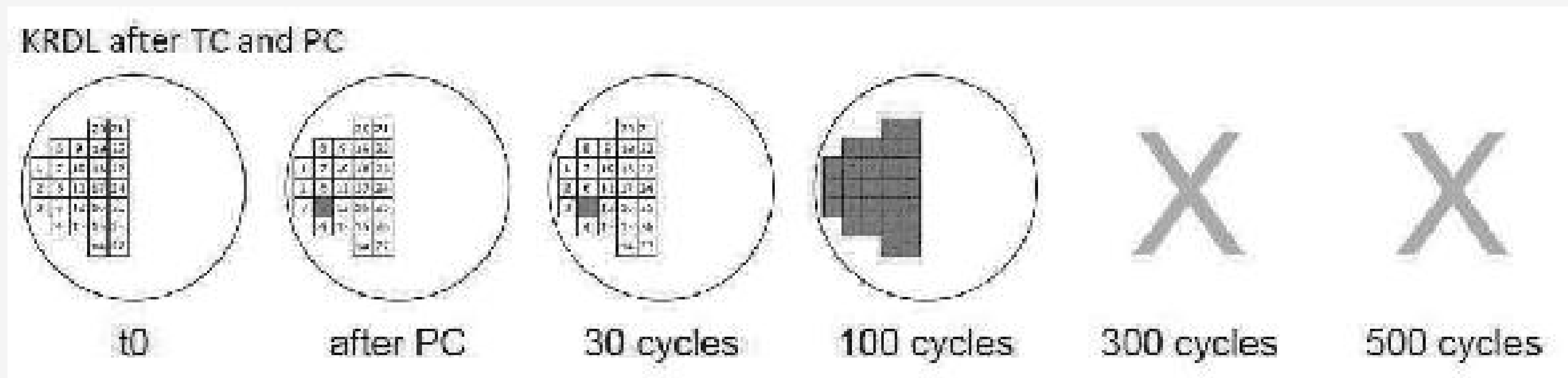
Reliability Test on 3DT1 W02 TSV



- HTS, 1000 hours @ +200C HTS test

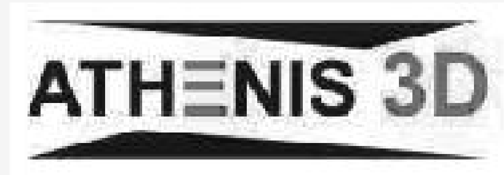


- TCY, 500 cycles after precon, range -65/+200C

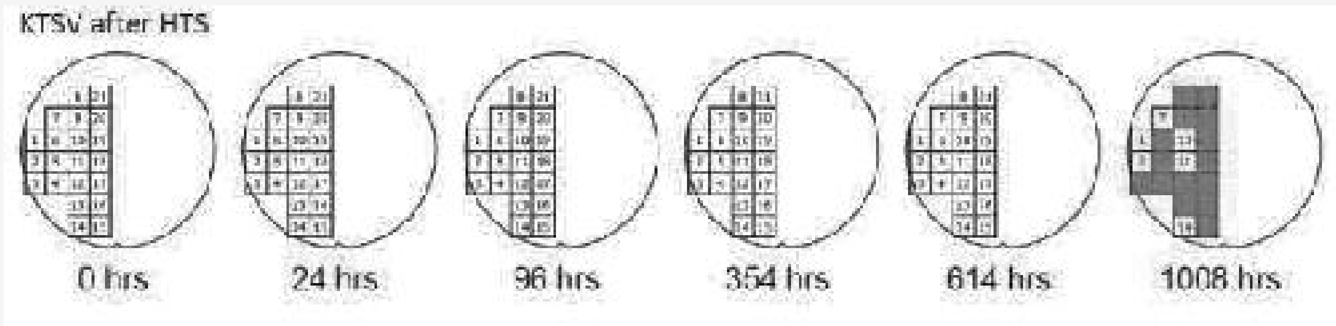


- 3DT1 w/o passivation failed TCY after 100 cy / HTS after 300 hr

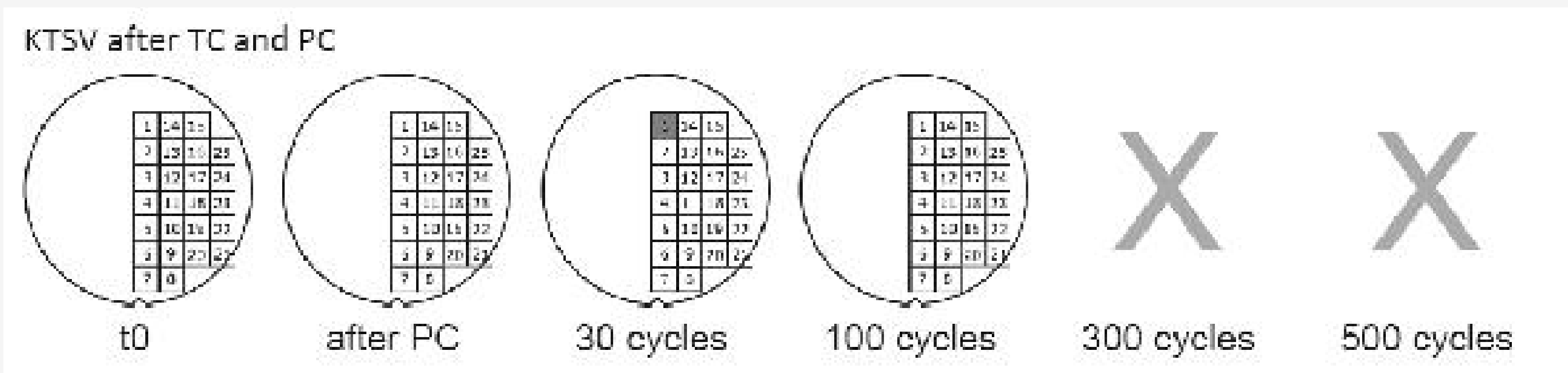
Reliability Test on Zibe W10 TSV



- HTS, 1000 hours @ +200C HTS test



- TCY, 500 cycles after precon, range -65/+200C



- Zibe cracked after 100 cycles

High Temp. Operating Life Test

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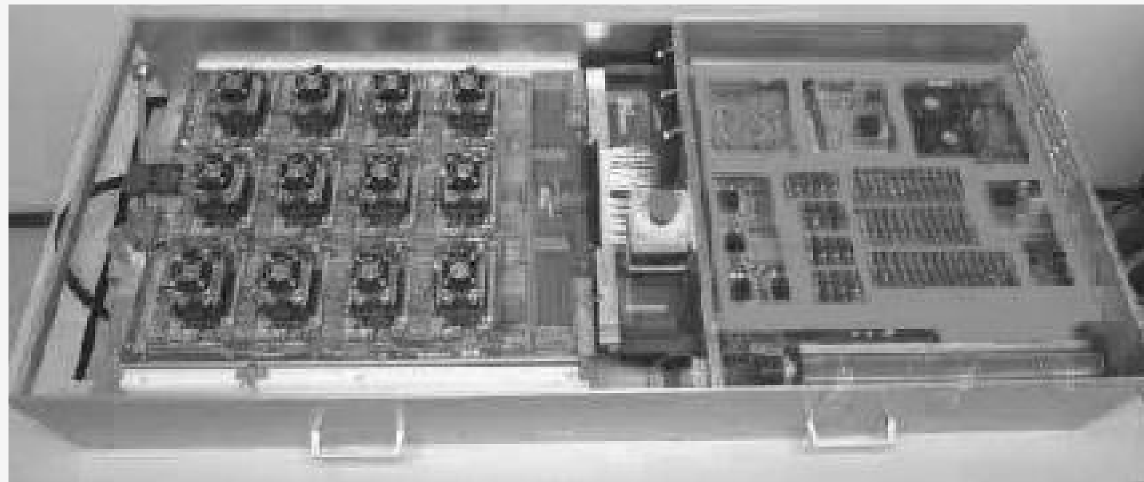
- 1000h HTOL test in progress, scheduled finish 7 April 2017
- Case temperature setpoint = 175°C
- Supply voltages set to 1.98 V and 1.1 V (10% above nominal)
- During the HTOL test 3 JTAG vector patterns are continuously being cycled
  - One cycle consists of 3 memory BIST patterns, named MARCH_LR, MARCH_M and MATS_PP. The TDO of each of the 12 DUTs is continuously monitored and matched with the expected pattern bit-by-bit.
- Interim readpoint result after 500h: 12 DUTs pass, no fails

Synergie CAD UDx700 development station

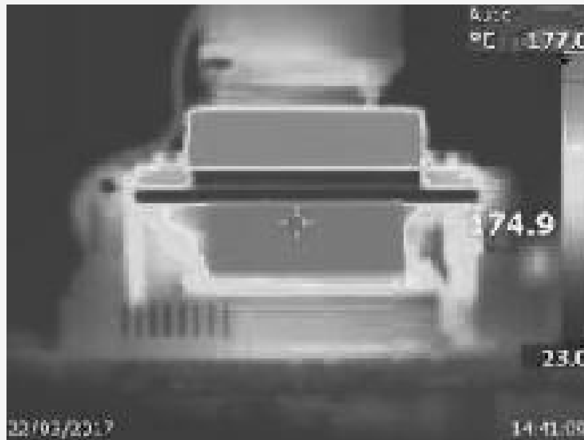
Left side: HTOL board

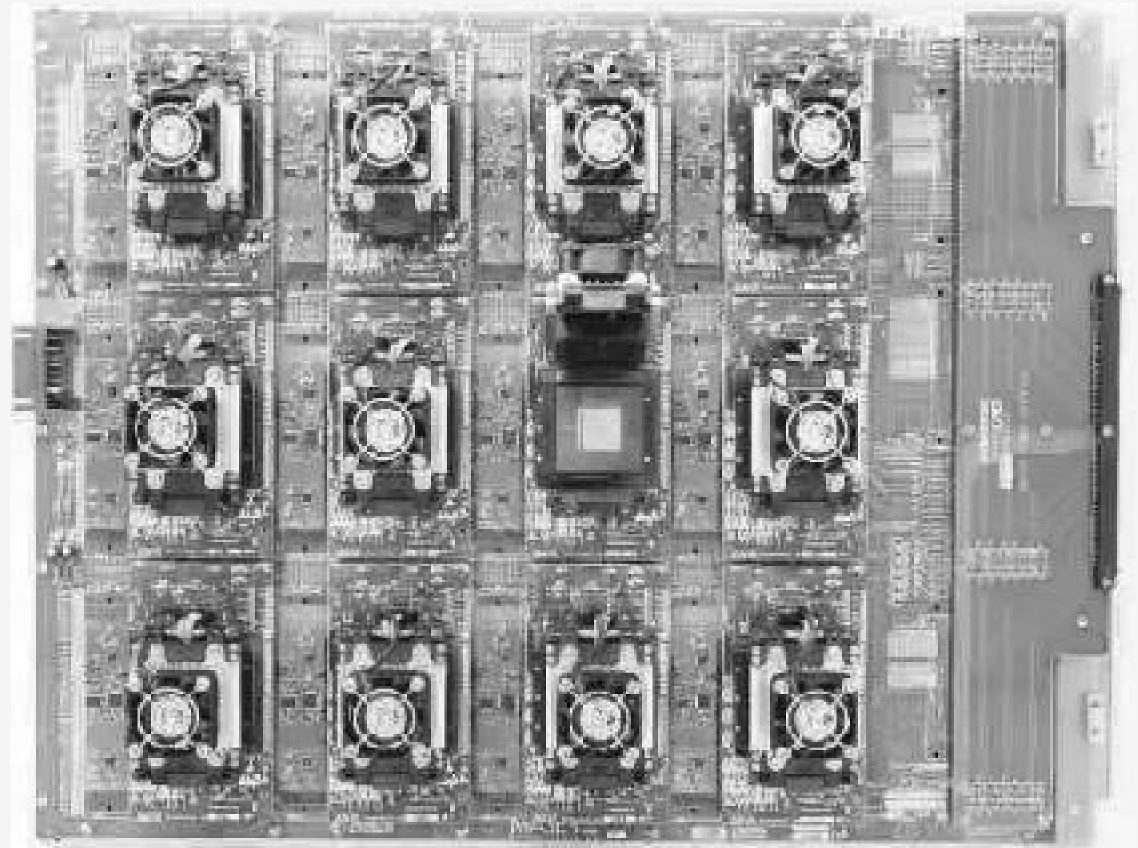
Right side: UDx700 driver



High Temp. Operating Life Test

- i-Socket™ based daughter card on main board





High Temp. Operating Life Test

ATHENIS 3D

- During the HTOL test 3 JTAG vector patterns are continuously being cycled. One cycle consists of 3 memory BIST patterns, named MARCH_LR, MARCH_M and MATS_PP. The TDO of each of the 12 DUTs is continuously monitored and matched with the expected pattern bit-by-bit.
- During the first 500 hours, 434055 cycles have been done.
- Pattern matching errors have been reported, on 4 DUTs only:
  - At cycle 100.078 an error was reported on DUT # C13 with the MARCH_M pattern.
  - At cycle 166.177 an error was reported on DUT # C10 with the MARCH_M pattern.
  - At cycle 288.933 an error was reported on DUT # C5 with the MARCH_LR pattern.
  - At cycle 414.209 an error was reported on DUT # C7 with the MARCH_LR pattern.

High Temp. Operating Life Test

- After 500 hours HTOL an interim readpoint was carried out by FHG IIS. All samples passed the functional test.
- Apparently device # C6 is still working fine despite the increased 1V1 current between 55 and 120 hours.
- The pattern matching errors on DUTs # C5, C7, C10 and C13 will be neglected, because the samples passed functional test and because the errors occurred only once during 500 During the 2nd 500 hours of HTOL testing, no pattern matching errors have been detected.
- After 1000 hours HTOL a final readpoint was carried out by FHG IIS. Again all samples passed the functional test.

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High Temp. Operating Life Test

ATHENIS 3D

The acceleration factor A can be calculated with the Arrhenius equation (1), with E_{aa} the apparent activation energy (2) and k the Boltzmann's constant (3).

$$A = e^{\frac{E_{aa}}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)} \tag{1}$$

$$E_{aa} = 0.7\ eV \tag{2}$$

$$k = 8.62 \cdot 10^{-5}\ {}^{eV}/_{K} \tag{3}$$

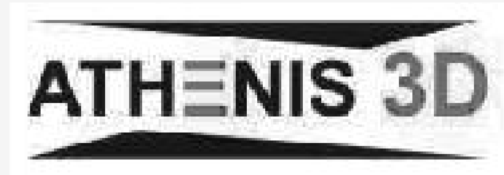
E_{aa} = 0.7 eV is a common rule of thumb for operational life testing.

The test duration can be reduced with a factor of 2.92 when the temperature is increased from 150°C to 175°C (4). The test duration can be furthered reduced with a factor of 2.61 when the temperature is further increased to 200°C (5). This results in a total acceleration factor of 7.62.

$$A = e^{\frac{E_{aa}}{k}\left(\frac{1}{150+273.15} - \frac{1}{175+273.15}\right)} \approx 2.92 \tag{4}$$

$$A = e^{\frac{E_{aa}}{k}\left(\frac{1}{175+273.15} - \frac{1}{200+273.15}\right)} \approx 2.61 \tag{5}$$

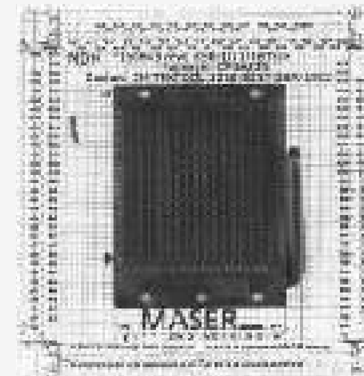
High Temp. HBM ESD Test



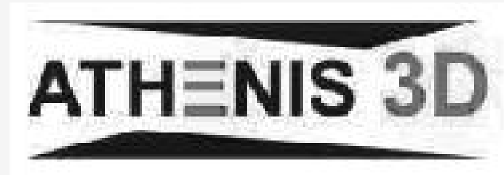
- HBM ESD test in progress, scheduled finish 7 April 2017
- HBM ESD evaluation at RT, 125°C and 200°C
  - 4 devices per temperature
  - 1 device: Complete ESD spiral from 500V until failure in 500V incremental steps
  - 2 devices: Last passing level (from spiral) until failure in 500V incremental steps
  - 1 device: Tested at last passing level -> to be subjected for final readpoint
- Preliminary failing levels

Temperature	1 Device: Spiral: 500V – Fail 500V steps	2 Devices: @ Last passing level – Fail 500V steps	1 Device: @ Last Passing level
Room Temperature	7000V	7000V/7000V	-
125°C	6500V	6500V/-	-
200°C	-	-/-	-

Mk.2 ESD tester with
InTEST ATS-750-M-9
Left: HT ESD test interface
Right: 200°C Thermostreamer setup



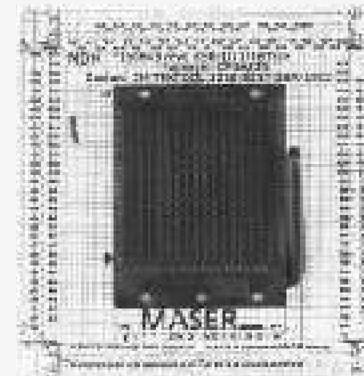
High Temp. HBM ESD Test



- HBM ESD test in progress, scheduled finish 7 April 2017
- HBM ESD evaluation at RT, 125°C and 200°C
  - 4 devices per temperature
  - 1 device: Complete ESD spiral from 500V until failure in 500V incremental steps
  - 2 devices: Last passing level (from spiral) until failure in 500V incremental steps
  - 1 device: Tested at last passing level -> to be subjected for final readpoint
- Preliminary failing levels

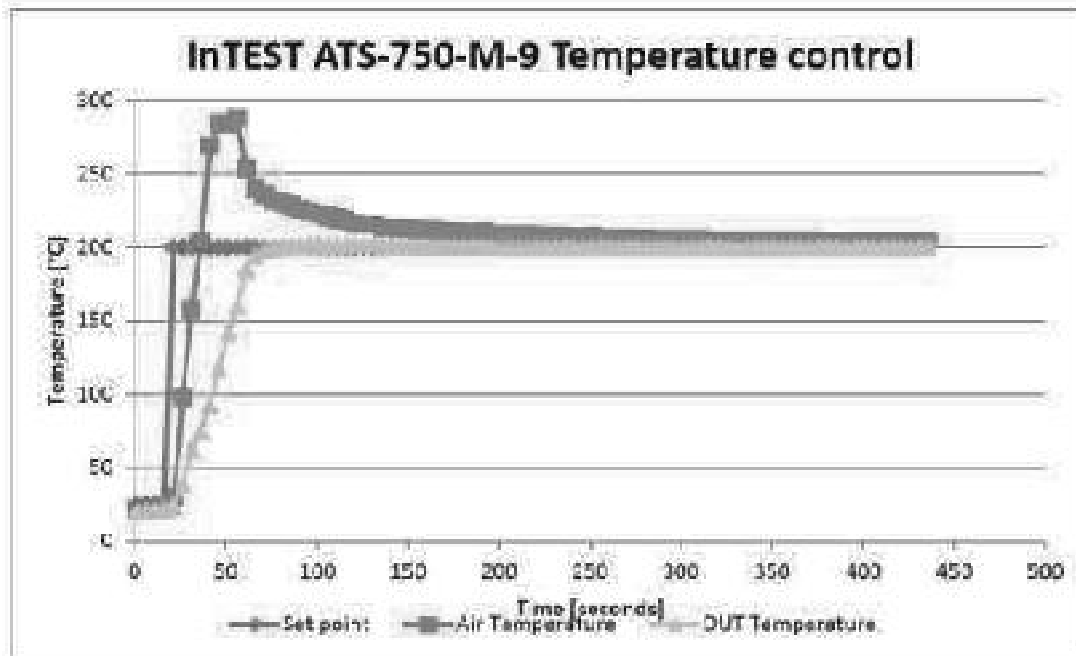
Temperature	1 Device: Spiral: 500V – Fail 500V steps	2 Devices: @ Last passing level – Fail 500V steps	1 Device: @ Last Passing level
Room Temperature	7000V	7000V/7000V	-
125°C	6500V	6500V/-	-
200°C	-	-/-	-

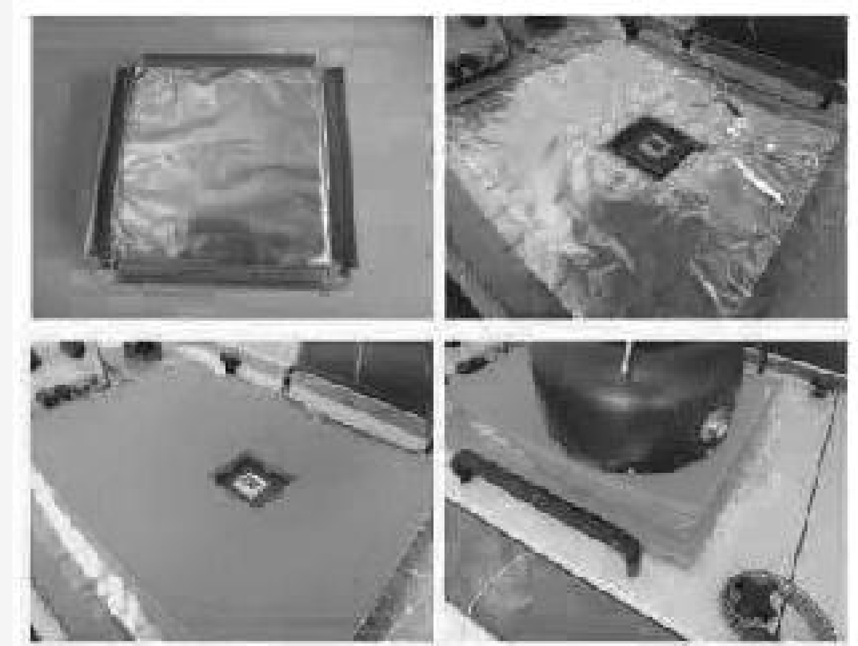
Mk.2 ESD tester with
InTEST ATS-750-M-9
Left: HT ESD test interface
Right: 200°C Thermostreamer setup



High Temp. HBM ESD Test

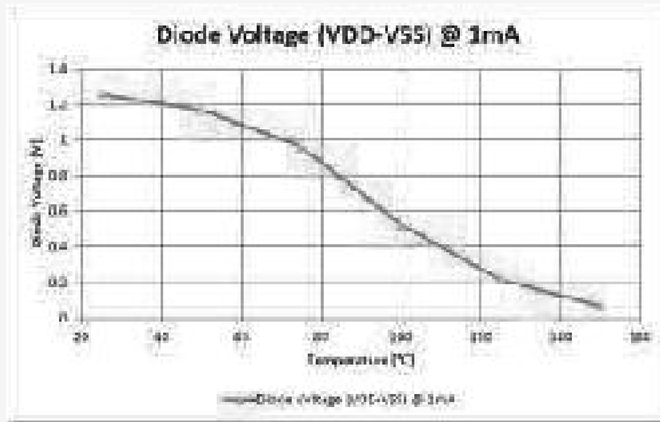
- **ESD test interface protection**
  - High temperature interface protection → stacked barriers silicone foam + Al foil
  - Low temperature interface protection to avoid condensation → closed interface PCB
  - Multi point thermal measurement nodes

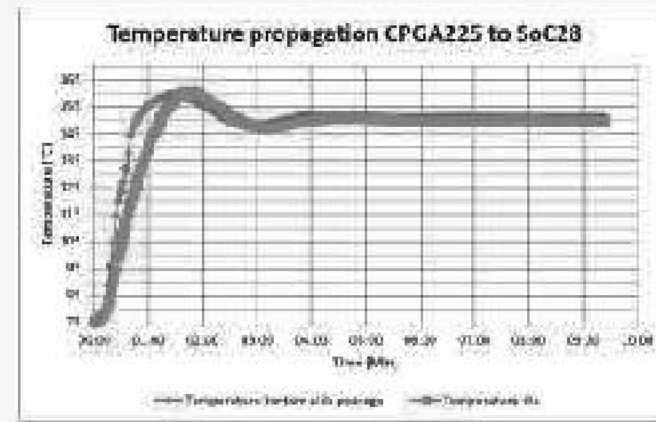


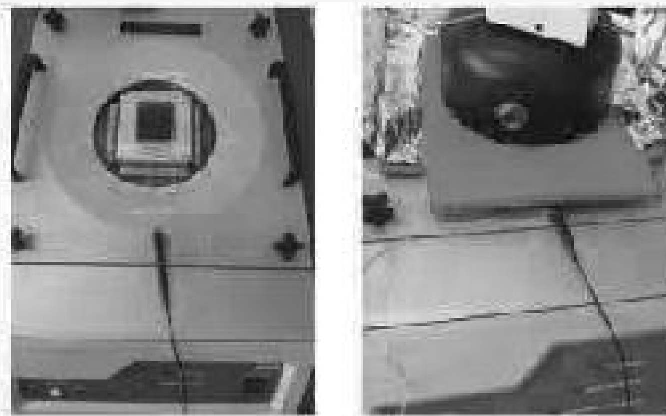


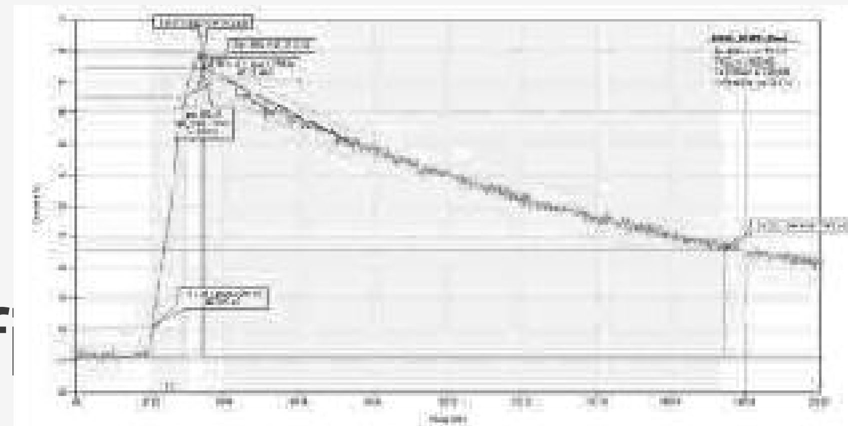
High Temp. HBM ESD Test

- On chip diode to measure chip vs package









High Temp. HBM ESD Test

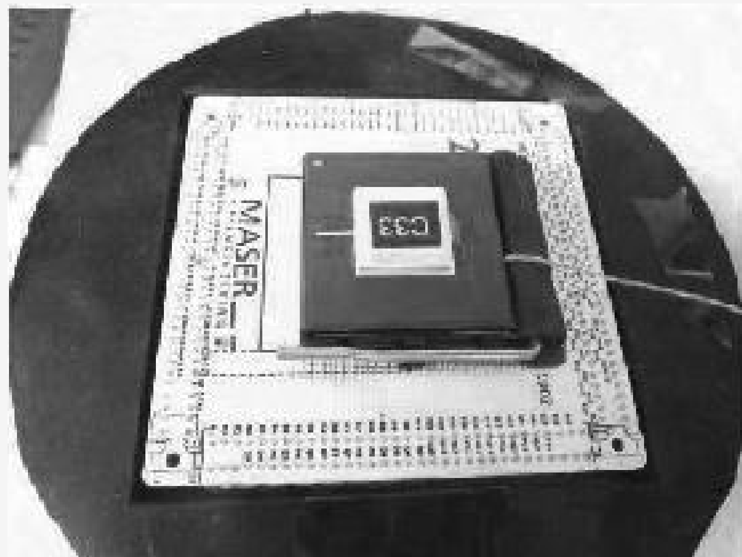
- ESD HBM test according AEC-Q100-002 E

Model	Standard	Voltages (V)	No. devices
HBM	AEC-Q100-002 REV-E	500 V .. Fail, step 500 V	1 (@ RT)
		Pass level .. Fail, step 500 V	2 (@ RT)
		Pass level previous ESD test for ATE	1 (@ RT)
		500 V .. Fail, step 500 V	1 (@125 °C)
		Pass level .. Fail, step 500 V	2 (@125 °C)
		Pass level previous ESD test for ATE	1 (@ 125 °C)
		500 V .. Fail, step 500 V	1 (@200 °C)
		Pass level .. Fail, step 250 V	2 (@200 °C)
		Pass Level previous ESD test for ATE	1 (@200 °C)

Table 6.2: ESD Voltage Test Sequence.

High Temp. HBM ESD Test

- **ESD test sequence**



Pin Combination Set Number [Note CC]	Pin(s) Connected to Terminal B (Ground)	Pins Connected to Terminal A (Single Pins tested one at a time)	Floating pins (No Connects)
1	DVSS	Every Supply Pin except pins of DVSS	All pins except PUT[1] and DVSS
		Every Non-Supply Pin	
2	VSS	Every Supply Pin except pins of VSS	All pins except PUT[1] and VSS
		Every Non-Supply Pin	
3	DVDD	Every Supply Pin except pins of DVDD	All pins except PUT[1] and DVDD
		Every Non-Supply Pin	
4	VDD	Every Supply Pin except pins of VDD	All pins except PUT[1] and VDD
		Every Non-Supply Pin	
5	VSSA0	Every Supply Pin except pins of VSSA0	All pins except PUT[1] and VSSA0
		Every Non-Supply Pin	
6	VSSA1	Every Supply Pin except pins of VSSA1	All pins except PUT[1] and VSSA1
		Every Non-Supply Pin	
7	VDDA0	Every Supply Pin except pins of VDDA0	All pins except PUT[1] and VDDA0
		Every Non-Supply Pin	
8	VDDA1	Every Supply Pin except pins of VDDA1	All pins except PUT[1] and VDDA1
		Every Non-Supply Pin	
9	All other Non-supply pins collectively except PUT	Each Non-supply pin, one at a time	All power pins

[1] Pin Under Test

Table 6.3: Pin Combinations (Table 2B, AEC-Q100-002)

High Temp. HBM ESD Test

Device	Stress Voltage	Combination	Stress Pins/Groups	Result	Remarks [2]
C32	500	1 – 9	All [1]	Pass	-
C32	1000	1 – 9	All [1]	Pass	-
C32	1500	1 – 9	All [1]	Pass	-
C32	2000	1 – 9	All [1]	Pass	-
C32	2500	1 – 9	All [1]	Pass	-
C32	3000	1 – 9	All [1]	Pass	-
C32	3500	1 – 9	All [1]	Pass	-
C32	4000	1 – 9	All [1]	Pass	-
C32	4500	1 – 9	All [1]	Pass	-
C32	5000	1 – 9	All [1]	Pass	-
C32	5500	1 – 9	All [1]	Pass	-
C32	6000	1 – 9	All [1]	Pass	-
C32	6500	1 – 9	All [1]	Pass	-
C32	7000	1 – 9	All [1]	Fail	[illegible] [3]
C33	6500	1 – 9	All [1]	Pass	-
C34	7000	1 – 9	All [1]	Fail	[illegible]
C37	6500	1 – 9	All [1]	Pass	-
C37	7000	1 – 9	All [1]	Fail	[illegible]
C14	6500	1 – 9	All [1]	Pass	For ATE test

Note [1]: All pins

Note [2]: [illegible]

Note [3]: [illegible]

Table 6.4: Analysis results ESD HBM test @ RT.

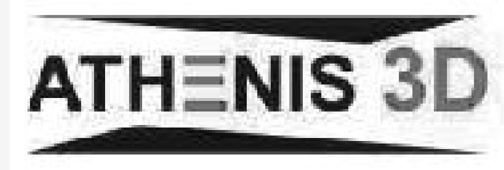
Device	Stress Voltage	Combination	Stress Pins/Groups	Result	Remarks [2]
C36	500	1 – 9	All [1]	Pass	-
C35	1000	1 – 9	All [1]	Pass	-
C35	1500	1 – 9	All [1]	Pass	-
C35	2000	1 – 9	All [1]	Pass	
C35	2500	1 – 9	All [1]	Pass	-
C34	3000	1 – 9	All [1]	Pass	[illegible]
C31	3500	1 – 9	All [1]	Pass	
C34	4000	1 – 9	All [1]	Pass	-
C30	4500	1 – 9	All [1]	Pass	
C31	5000	1 – 9	All [1]	Pass	
C30	5500	1 – 9	All [1]	Pass	[illegible]
C30	6000	1 – 9	All [1]	Fail	[illegible]
C40	5500	1 – 9	All [1]	Pass	
C41	6000	1 – 9	All [1]	Fail	[illegible]
C42	5500	1 – 9	All [1]	Pass	
C42	6000	1 – 9	All [1]	Fail	[illegible]
C45	5500	1 – 9	All [1]	Pass	For ATE test

Note [1]: All pins

Note [2]: [illegible]

Table 6.6: Analysis results ESD HBM test @ +200 °C.

High Temp. HBM ESD Test



ESD Test Voltage	RT	+125 °C	+200 °C
500 - 5000	1/1	1/1	1/1
5500	1/1	3/3 + (1/1) [1]	3/3 + (1/1) [1]
6000	1/1	2/3	0/3
6500	3/3 + (1/1) [1]	0/2 [2]	-
7000	0/3	-	-

Note [1]: Tested at last pass level and ATE (Pass ATE/Tested)
Note [2]: Only 2 devices tested because one device was already failing at 6000 V

Table 6.7: Overall ESD result (Pass/Tested).