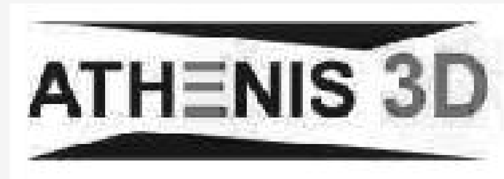
ATHENIS 3D

WP6: PROCESS AND PLATFORM INTEGRATION

Leader:	**ams AG – Jörg Siegert**
Start:	M9
End:	M40

WP6 planned effort and Deliverables



Planned Efforts after updated DoW

Work package		AMS	VEEM	Crocus	FHG	TUW	UNIFE	AT	MASER	BESI	CEA	UNIPI	Total
WP6	Planned person.months per participant	**22.0**	13.0	**2.0**	3.0	3.0				10.0	3.0		**56.0**
	Actuals	**31.7**	13.0	**2.8**	3.0	3.5				10.1	1.0		**65.1**

Deliverables

D6.1: M12 ✓ Report on 3D integration concepts [AMS]
D6.2: M29 ✓ Report on Manufacturing technology flow for WLP [BESI]
D6.3: M27 ✓ Report on HVCMOS interposer manufacturing technology flow [AMS]
D6.4: M40 ✓ Report on Evaluation of costs and manufacturability of the ATHENIS_3D technology platform [AMS]
D6.5: M27 ✓ Specification and commitment done for type of Demo Car [VES]

Milestone

MS4 M18 ✓ Specification and commitment done for type of Demo Car [VES]

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WP6: T6.1 Definition of 3D integration concepts

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Overview:

- Define integration concepts for the AMS HVCMOS interposer with Cu TSV, Power Cu RDL, CROCUS eNVM MRAM and IPDs

Challenges:

- Extreme requirements for very low On-resistance R_{on} for the H-bridge driver application → thick metallization (≥150 µm) required → use DBC on ceramic substrate
- Wide range of operating requirements (e.g. high/low current, high/low density of interconnects, …) → evaluate components

Highlights:

- 3D integration concepts worked out together with partners and summarized in D661

WP6: T6.2 Process integration flow development for WLP

Overview:

- Evaluation of suitable D2W stacking approaches suitable for applications in harsh environments

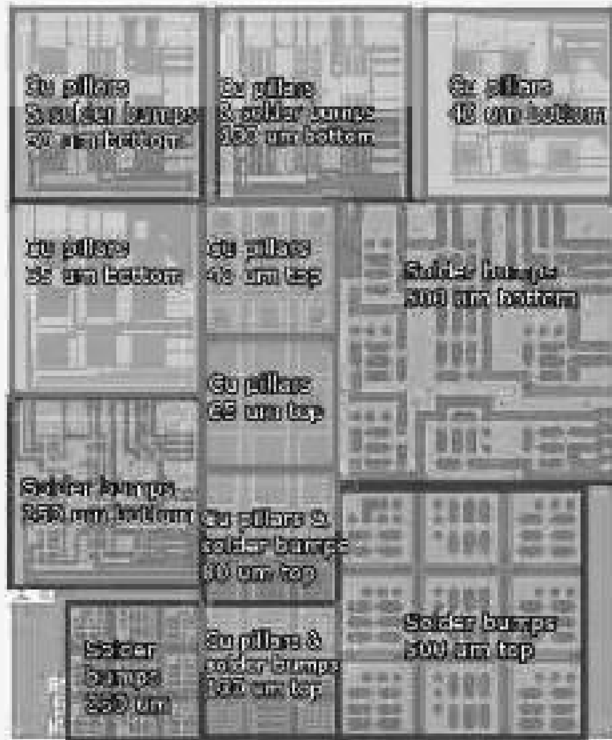
Challenges:

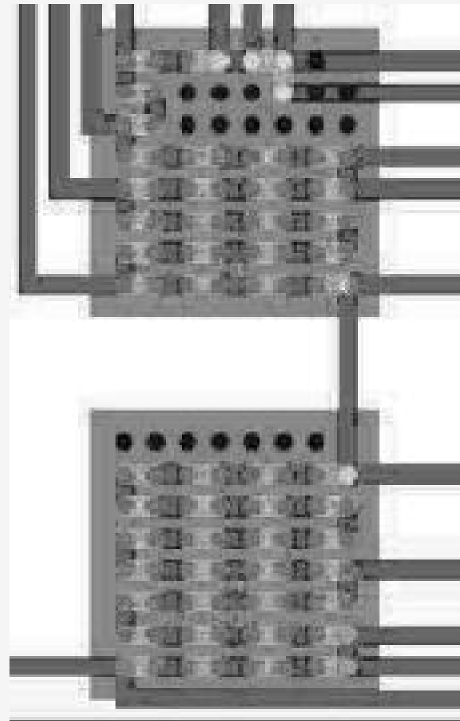
- Pushing solder ball pitch beyond state-of-the art
- Low yield of samples after balling

Highlights:

- Manufacturing and successful electrical characterization (incl. reliability tests)
- D2W stacking of samples with 20 µm bump/40 µm pitch

D2W stacking





Test vehicle	Bump type	Bump diameter	Bump pitch	Stacking process	Purpose
TV 1	Cu-pillars	20µm	40µm	TCB	Evaluate TCB process
				C2	Pushing the pitch limits beyond state-of-the-art
TV 2	Cu-pillars	30µm	65µm	C2	Evaluate C2 process
				TCB	TCB and C2 process comparison
TV 3	Cu-pillars	40µm	80µm	C2	Comparison w/ TV 2
	Solder balls			C4	Pushing the pitch limits beyond state-of-the-art
TV 4	Cu-pillars	70µm	130µm	C2	Comparison w/ TV 2 and TV 3
	Solder balls			C4	TV 4 – C2 and C4 process comparison

D2W stacking – technology demonstrator

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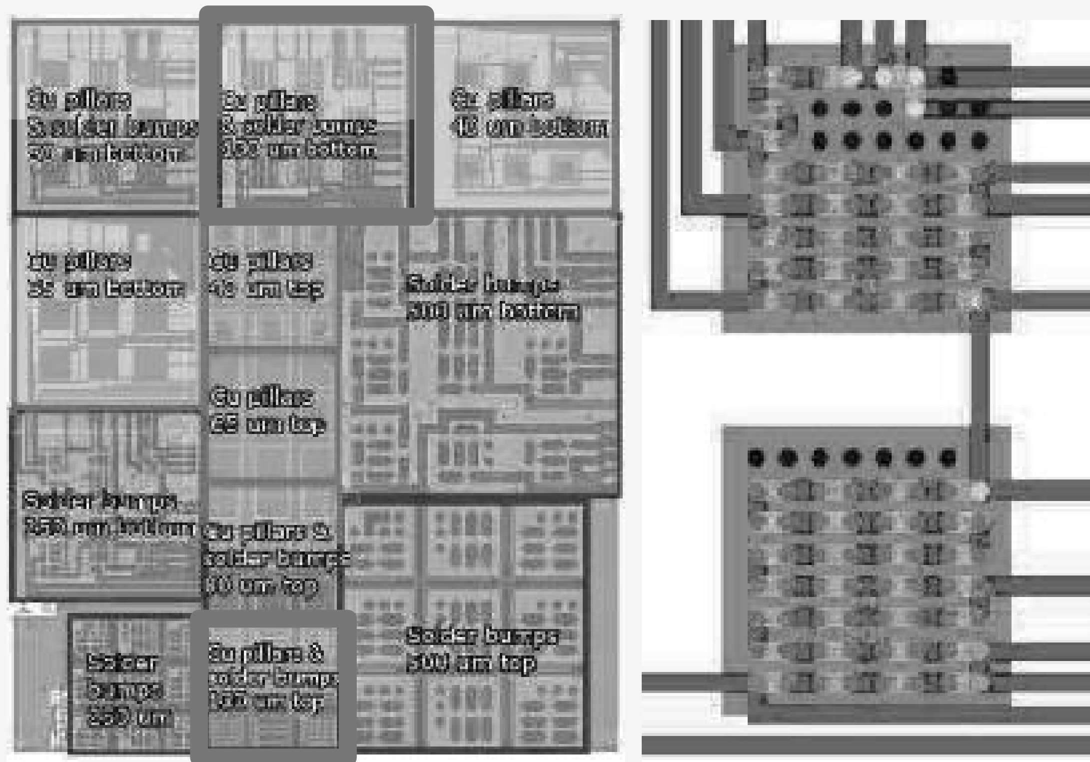

SoC: 165 µm pad pitch / 75 µm balls

TV4: 130 µm pad pitch / 70 µm balls (4.35 x 4.35 mm², 567 balls)

D2W stacking test chips

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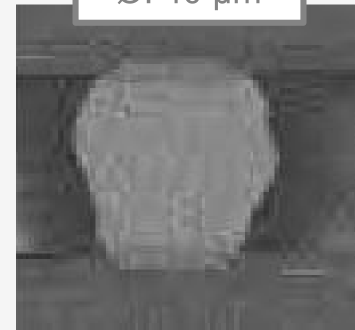
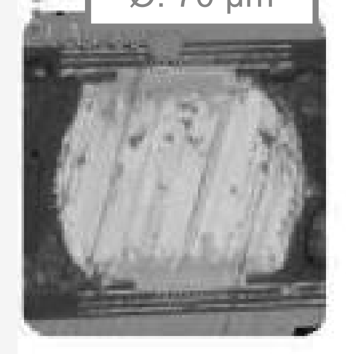
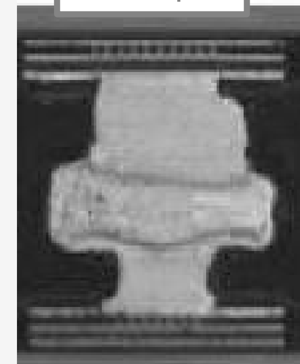
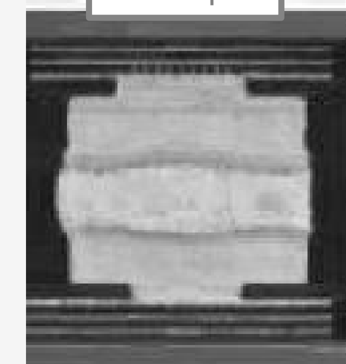
- Processed
  - Targeted interconnection with smallest diameter
    - Keep chip size small
    - Push limits of reflow process
  - Solder ball
    - Diameter: 40 & 70 µm
  - Copper pillar
    - Diameter: 20 & 30 µm

- Characterization done on all processed interconnections
- First reliability test done on solder balls with diameters of 70 µm









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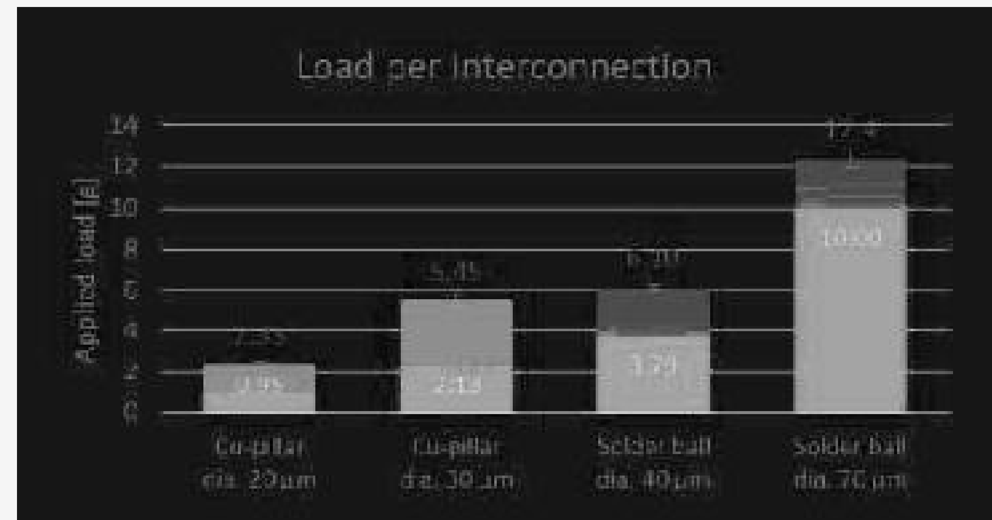
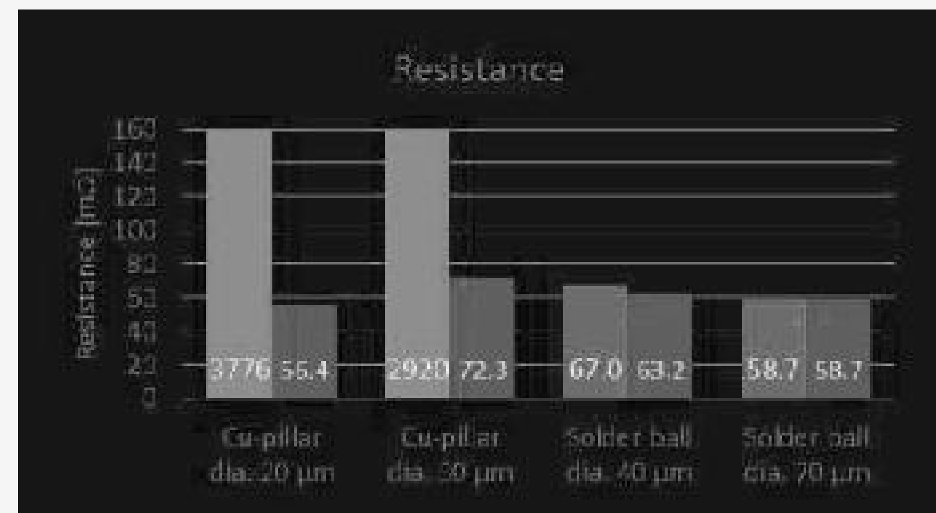
D2W stacking characterization

- Mechanical characterization
  - Shear test
  - Minimum load values according to BESI standard
  - ➔Stability increase with interconnect size



- Electrical characterization
  - Resistance of
    - single interconnection
    - Daisy chains of 49 and 97 interconnections
    - Compare to theoretical value
  - ➔Electrical connection achieved



WP6: T6.3 Development of HVCMOS interposer manufacturing technology flow including TSV and BRDL

Overview:

- Adaption of 3D flows for advanced technology nodes and automotive applications

Challenges:

- Process flow divided into different places (ams, CEALETI, BESI and subcon)
- Reliable manufacturing of prototypes

Highlights:

- Definition of requirements for WLOM and implementation
- Successful fabrication of technology demonstrators

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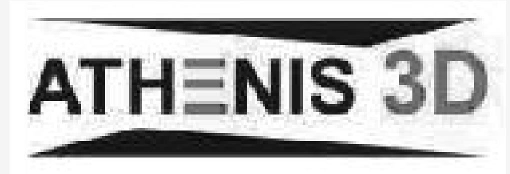
WP6: T6.4 Evaluation of costs and manufactu-rability of the ATHENIS_3D technology platform



Overview:

- Assessment of manufacturability of 3D integrated solutions
- Comparison of 3D integrated solution with traditional packaging (cost, form factor, performance)

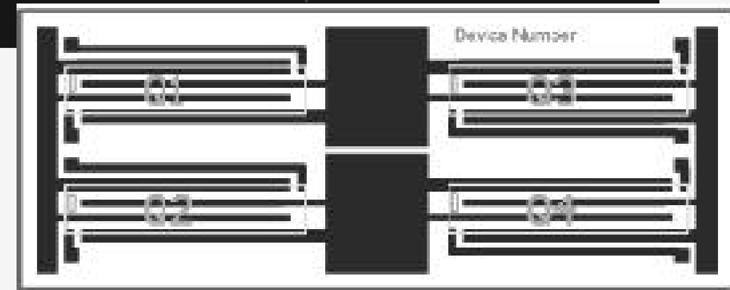
Challenges:

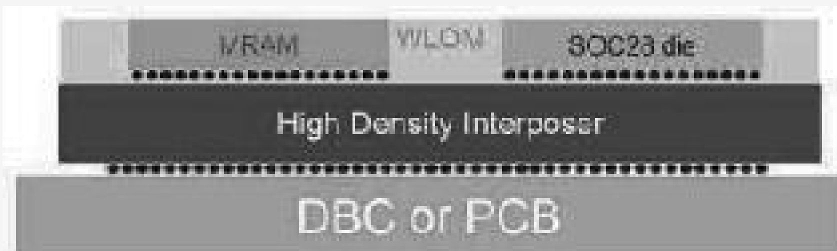
- Definition of the final flow
- Evaluation of impact when transferring from R&D to production

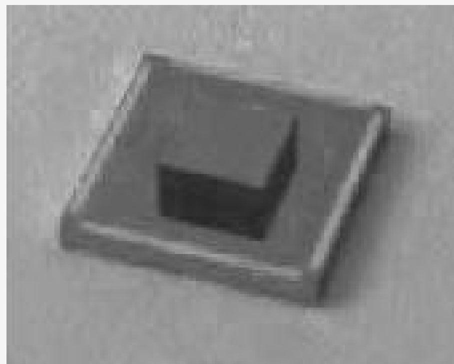
Highlights:

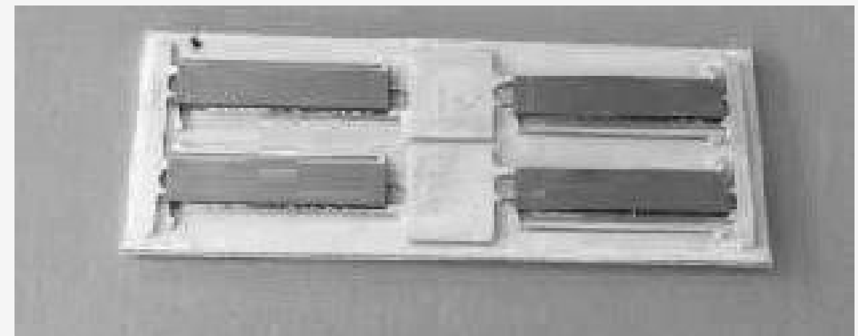
- 3D integrated solutions (slightly) more expensive but offer significant form factor advantages
- Yield allows for economically feasible production

Demonstrator









Integration modules

Device	technology	TSV	UBM	Balling	Stacking	WLOM	MRAM
passive HD Interposer	0.35µm 4M	✓	✓	✓ (1 side)	✓	✓	
DCDC	0.35µm HVCMOS						
H-bridge PMOS	0.35µm HVCMOS		✓	✓	✓		
H-bridge NMOS	0.35µm HVCMOS		✓	✓	✓		
Gate Driver	0.18µm HVCMOS		✓	✓	✓		
MRAM	0.18µm HVCMOS						✓
SoC28	28nm CMOS		✓	✓	✓		
Cap - IPD	based on TSV flow	✓					

Manufacturability

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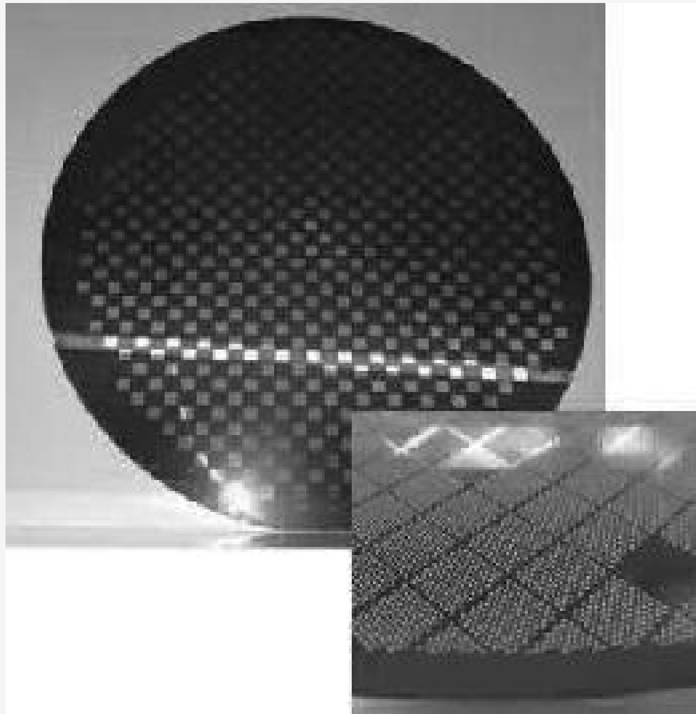
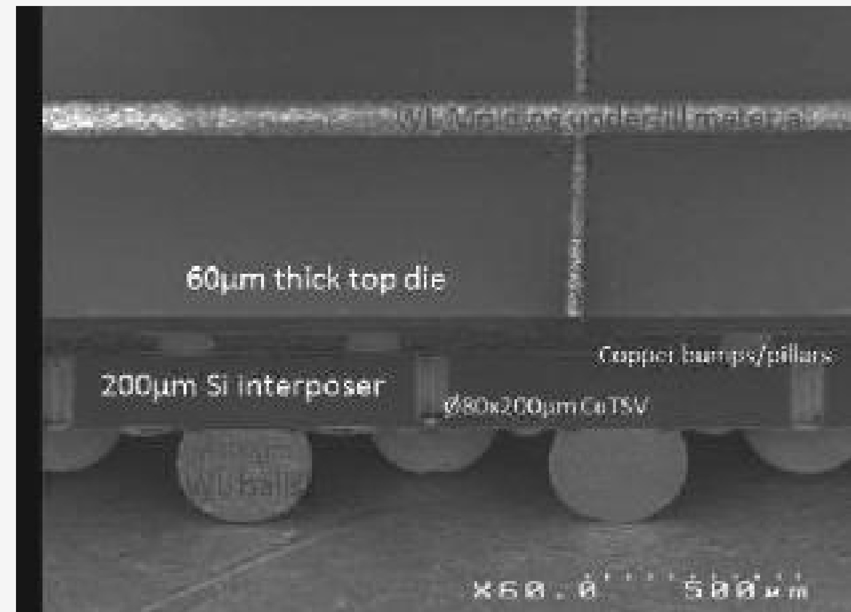
- Yield losses for wafer processing including 3D steps like TSV are considered both from the study cited in this report as well as from mature manufacturing point of view to be typically in the low %-range.
- System integration of prototypes as demonstrated in ATHENIS_3D with D2W stacking of high density I/O flip chip interconnects required optimization of the new modules (e.g. D2W, wire bonding on interposer) to bring the yield in 3 iterations from 10% to 60% to deliver a sufficient number of samples for the SoC28 characterization and reliability investigations.

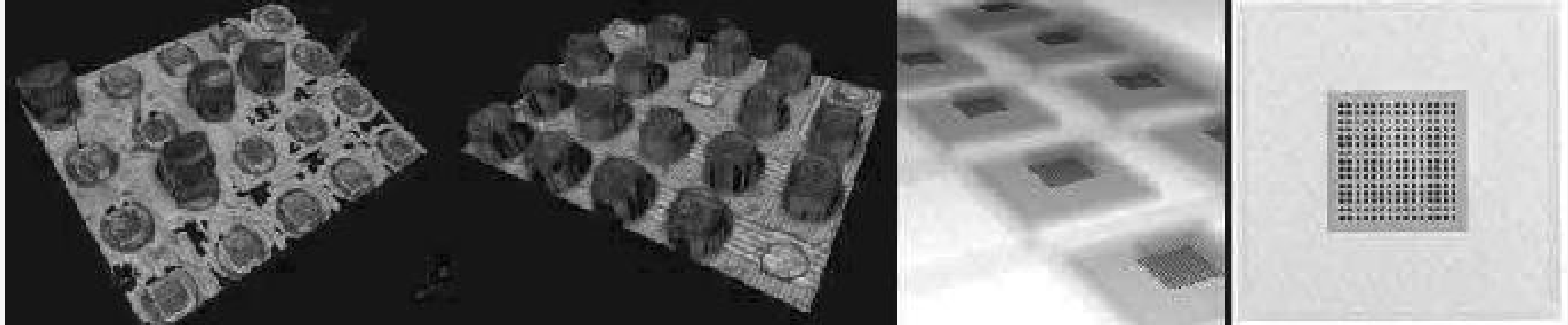
Integration TSV

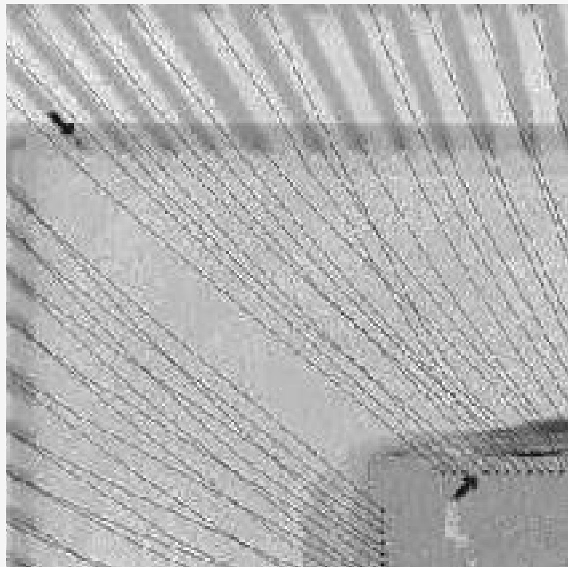




- TSV100/80 in high volume production (medical, consumer)
- Specific needs for ATHENIS_3D addressed
    - Cu TSV
    - WLOM (TSV → D2W stacking → WLOM → bumping)

Integration SoC28

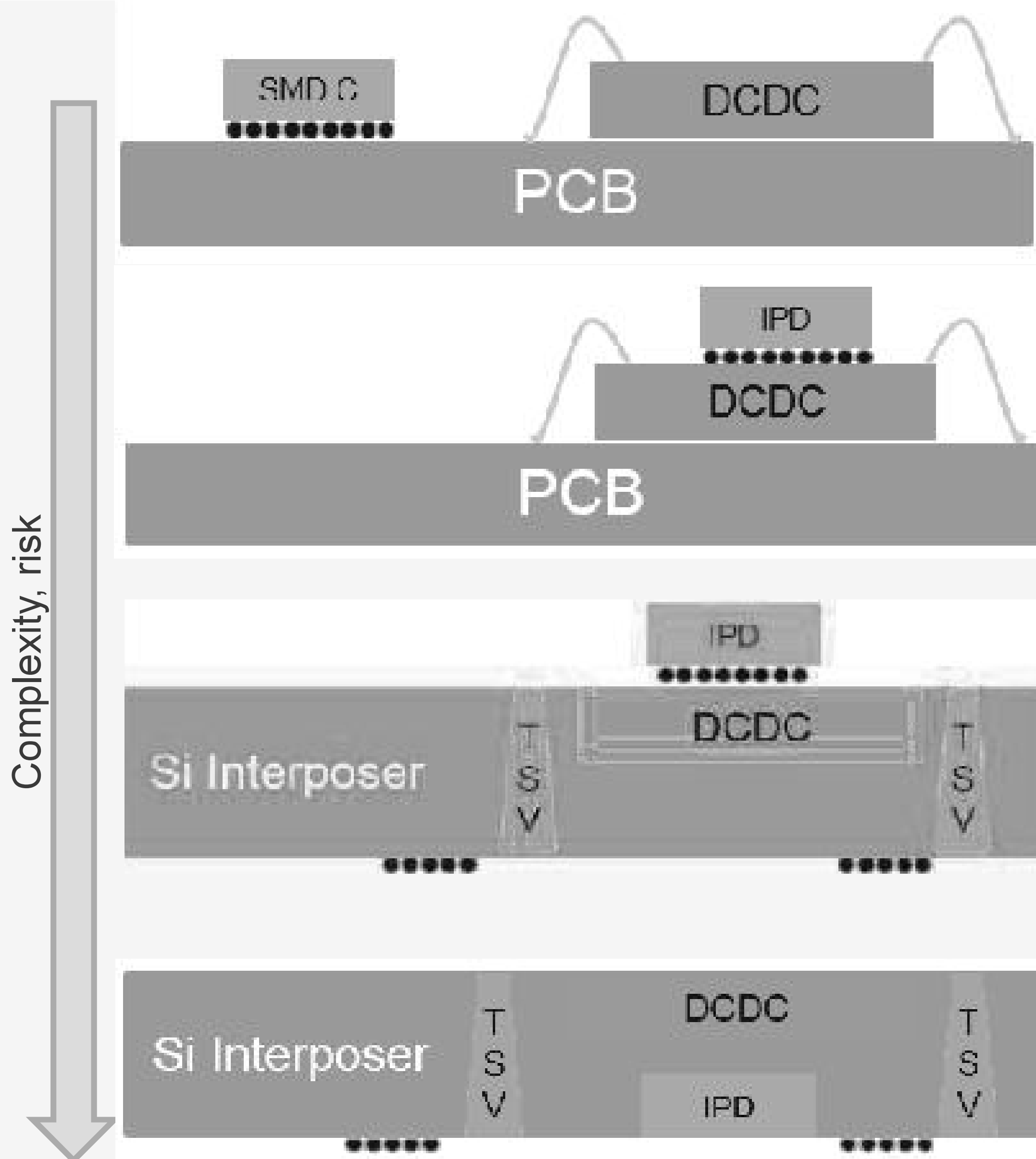




D2W stacking
- Initial samples mechanically ok but 15% opens (1st if each sample placed on substrate w/o bonding)
- Software upgrade to correct issue

Wire bonding
- Problems at assembly (225 wire bonds to staggered leadframe)
- Additional iteration for improved yield

Cost IPD



Overall cost ~ +30%
No performance difference
Better cooling

Overall cost ~220%
Smaller possible form factor (space for additional chips on interposer)

Overall cost ~220%
Smallest possible form factor (space for additional chips on interposer)

Cost H-bridge

Standard driver: $0.762 per unit	==> 4 x drivers:	$3.128
Industrial MOSFET: $0.449 per unit	==> 4 x MOSFETS:	$1.796
	Total	**$ 4.924**

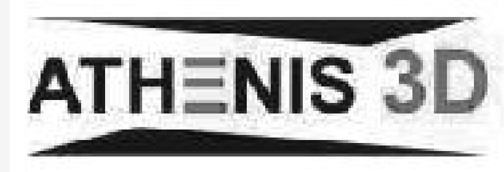
Device	price range	avg. price	total
NMOS 100mOhm	€ 1.00 – 1.20	€ 1.10 x2	€ 2.20
PMOS 100mOhm	€ 1.30 – 1.50	€ 1.40 x2	€ 2.80
Smart Driver	€ 1.80 – 2.00	€ 1.90 x1	€ 1.90
		Total	**€ 6.90**

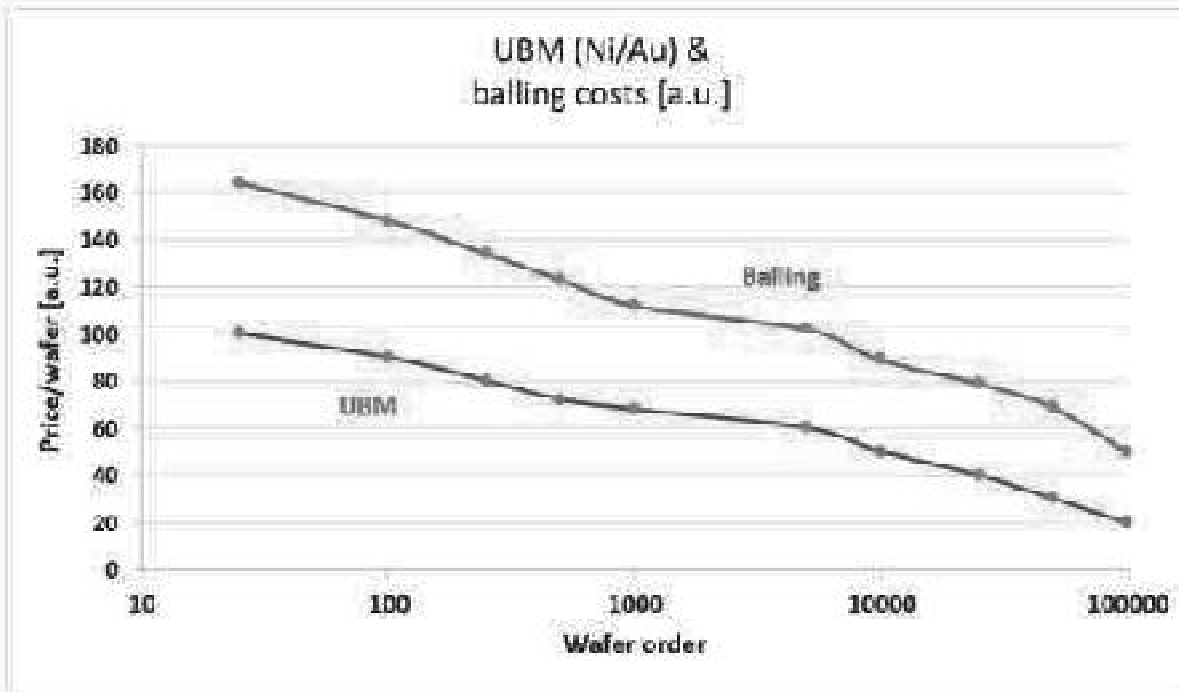
Area for R_{ON} ≤ 100mOhm @ 175 ° C

Advantages of integrated solution:

- Integration of a current mirror pad (actual current, voltage and temperature of the transistor)
- Reverse polarity protection (HV transistor concept)
- Advanced VDS loop, current switch control and extended safety functions (integrated driver IC)

Cost UBM, balling and stacking





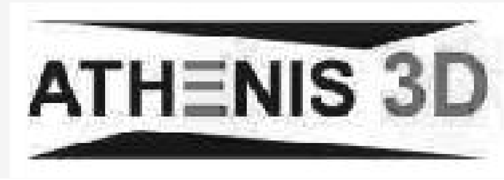
Subcontracted costs: UBM & balling

- Costs strongly dependent on volume
- Balling costs dominating

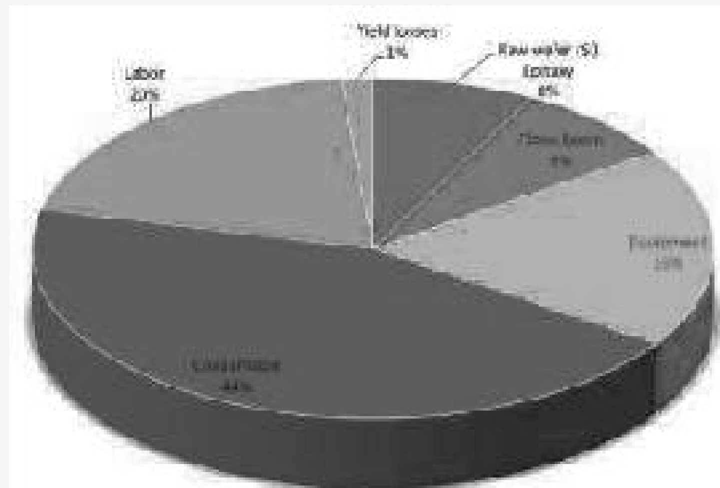
D2W System	CHAMEO advanced	TC advanced
accuracy	3µm	2µm
soldering	Dip fluxing + general reflow	TC local reflow
uph	4500	1000
cost/bond (~€ ct) relative units	1	7x

D2W stacking costs strongly dependent on soldering approach (C2/C4 vs. TCB)

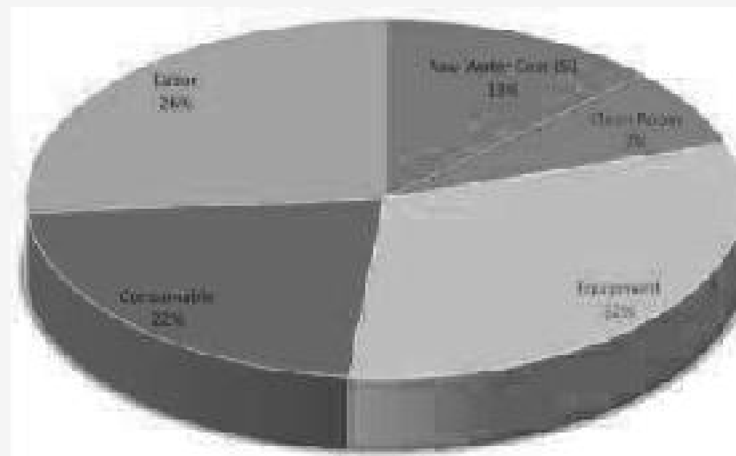
Cost contribution CMOS and 3D (W TSV)



0.35µm HV CMOS



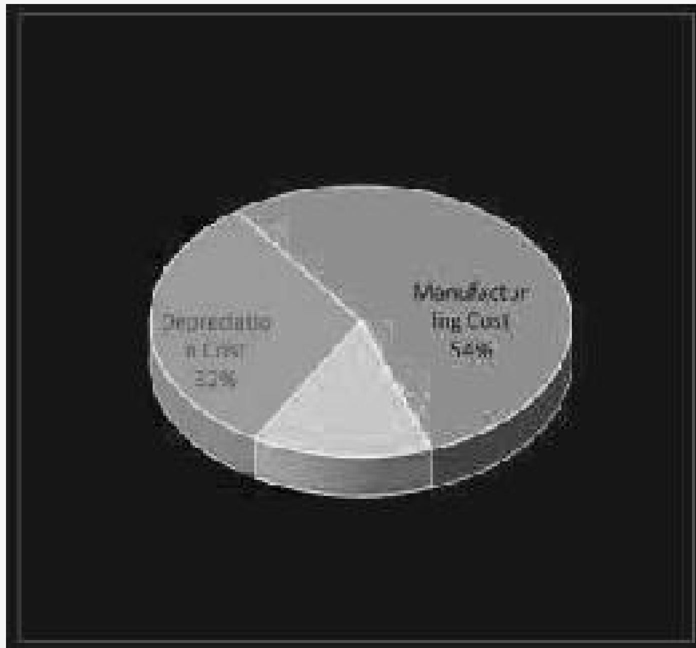
3D module ams (W TSV)

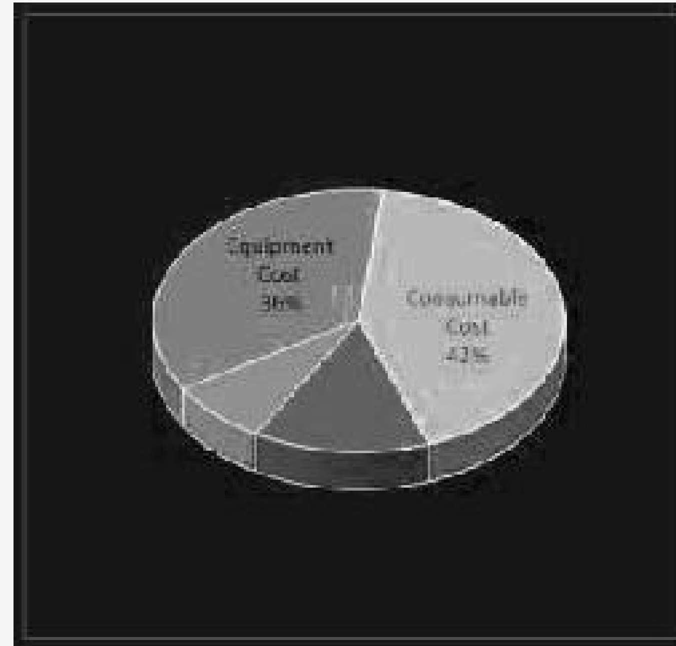


Technology	Wafer cost	TSV / BRDL	UBM	Balling	WLOM	MRAM
0.35µm HV CMOS	100%	75%	13%	23%		
0.18µm HV CMOS	155%	49%	9%	15%		14%
4M HD passive interposer + TSV + BRDL + UBM + WLOM + 1 side balling	169%					

Relative to base technology

Cost contribution 3D (Cu TSV)



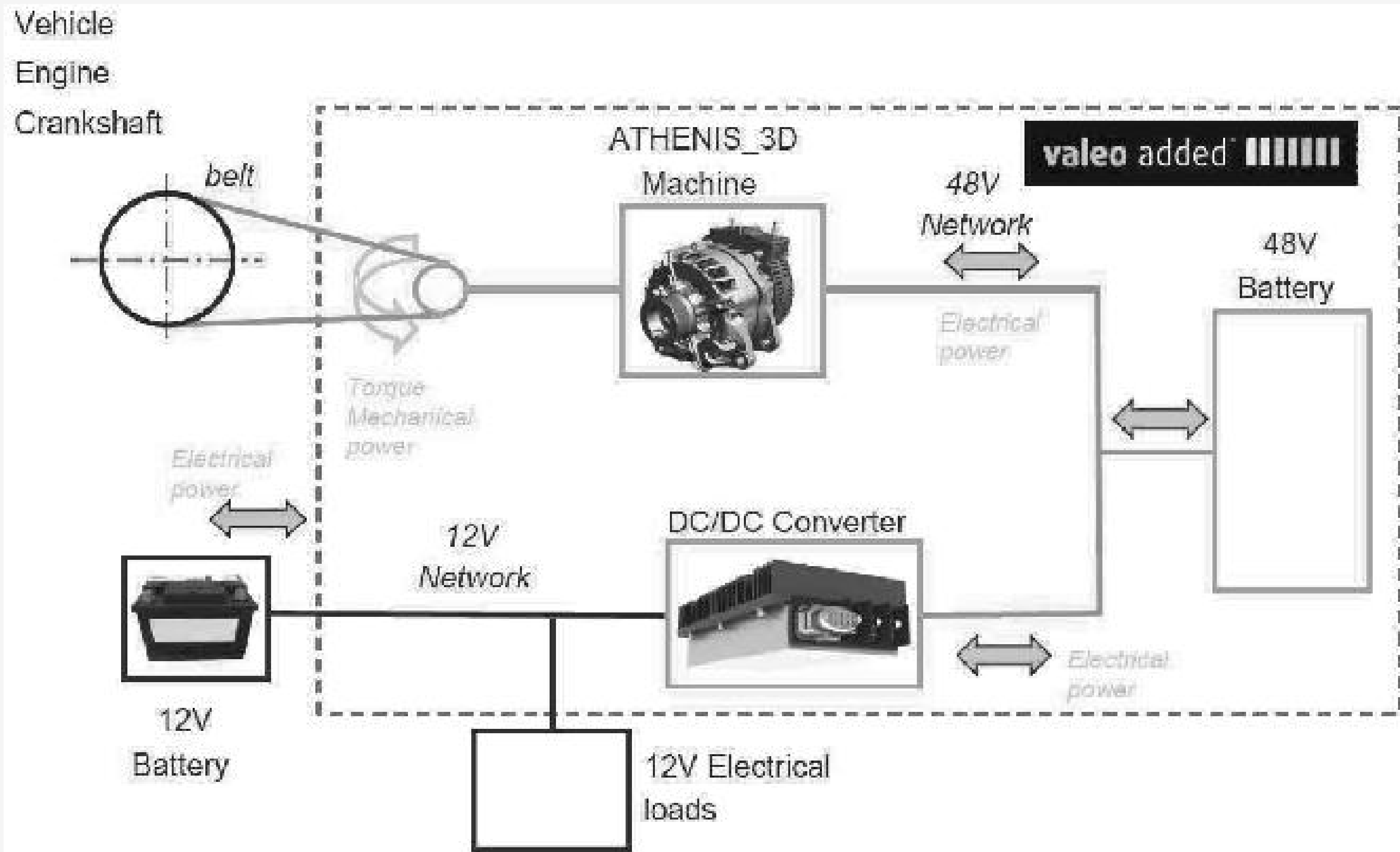


Slightly different numbers compared to ams

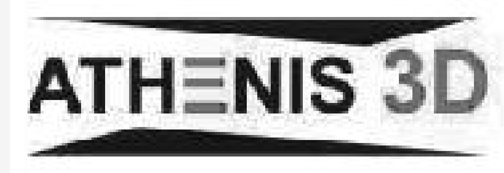
- Different process
- Not manufacturer

➔ potential to process Cu TSVs with improved resistance at same or lower manufacturing costs

D665: Electrical architecture



D665: Operational limits



Operating range	
Maximum ambient temperature	80℃
Maximum continuous rotational speed Permanent Alternator current on 48V side	16,000rpm 0 to 30A
Voltage regulation	54V+/-1V
Maximum rotor current	1.5A

The 48V alternator has been adapted specifically for ATHENIS_3D demonstrator

D665: Alternator control module

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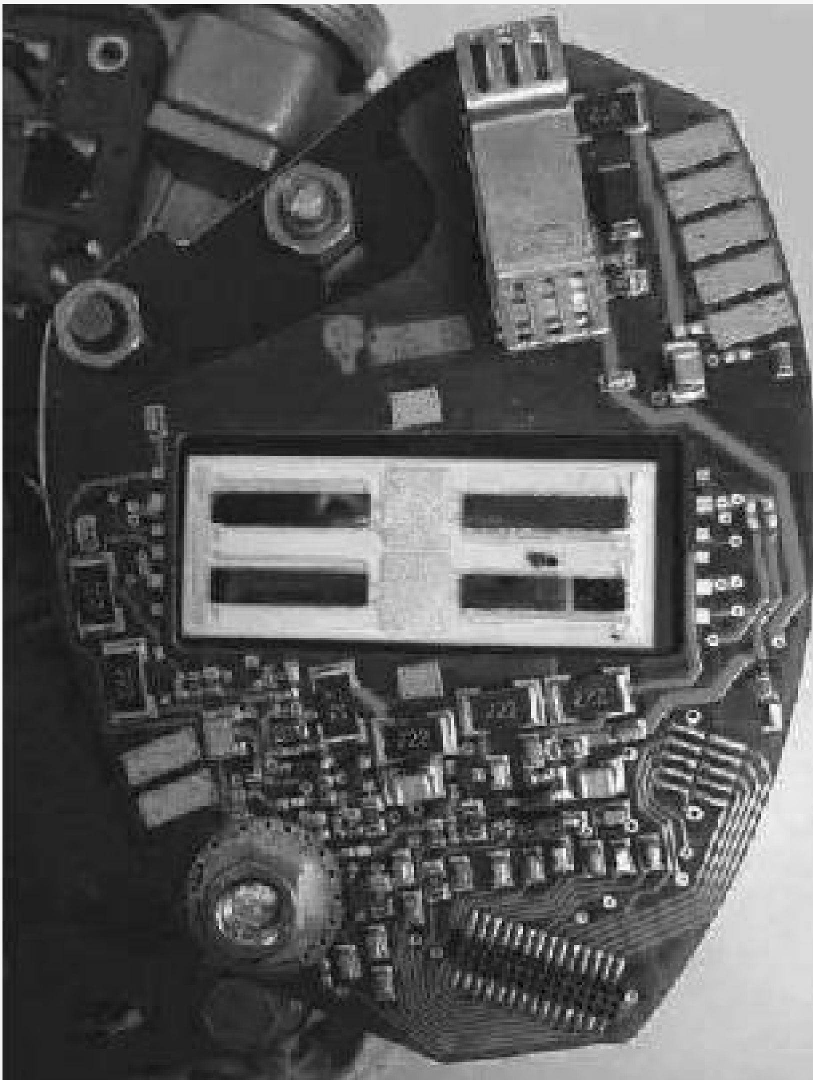
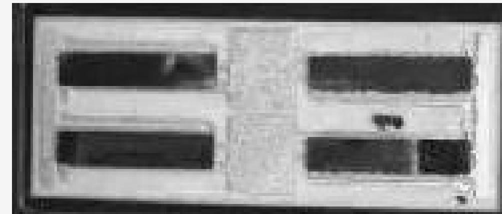
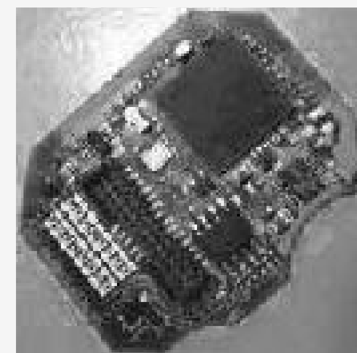




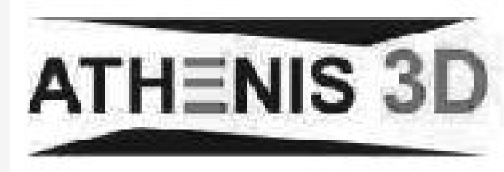
H-bridge
(HVCMOS on DBC)

Interface PCB
(includes drivers for H-bridge)

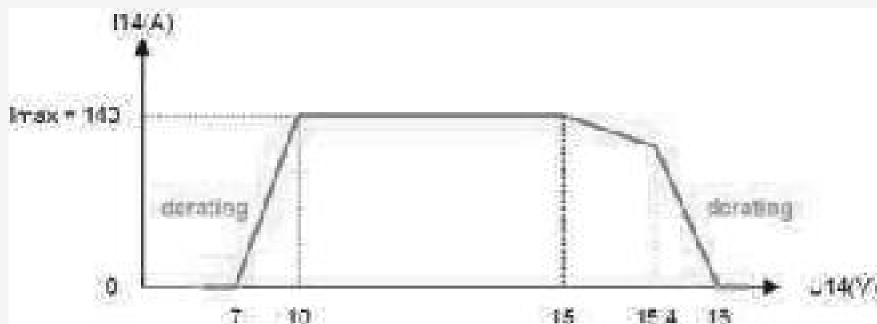


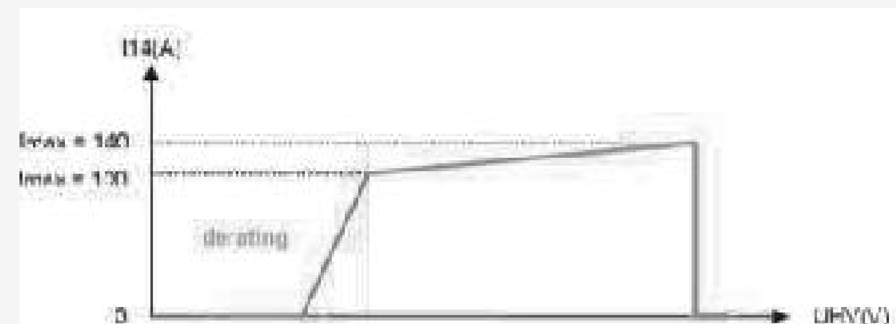
Fast prototyping module

D665: DCDC converter requirements

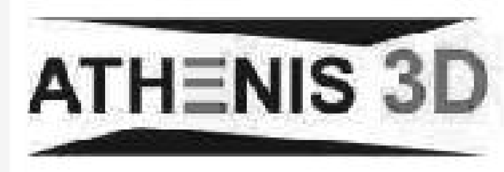


- output power between −30°C and +70°C
  : 2.0kW @ U14 = 14V
- air cooled : 4 × regulated fans, better with airflow
- efficiency : Efficiency higher than 75% for output power between 10% and 50%
  Efficiency higher than 85% for output power between 50% and 100%
- power architecture : 4 × 500W power cells in parallel
- control : CAN high-speed (500kbits/s)





D665: System wiring for prototype



48V battery

12V Network

Battery Positive cable

12V Battery

HV GND

DC/DC Converter

12V Ground

HV Network

HV Ground

HV Network

ATHENIS_3 D Alternator

HV Ground (Bracket link, no cable)

D665: Functional mode evaluation

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Cranking by conventional starter → all signals measurement

Idle speed regulation at 48V → 48V and 12V voltage measurements

Idle speed regulation at 48V versus loads → 12V and 48V voltage and current measurements

Idle speed regulation at 48V versus switched loads → 12V and 48V voltage and current measurements

48V regulation versus speed/loads/switching → 12V and 48V voltage and current measurements

12V regulation versus 48V variation (large signal) → 48V and 12V voltage measurements

Driving measurements → 12V and 48V voltage and current measurements

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